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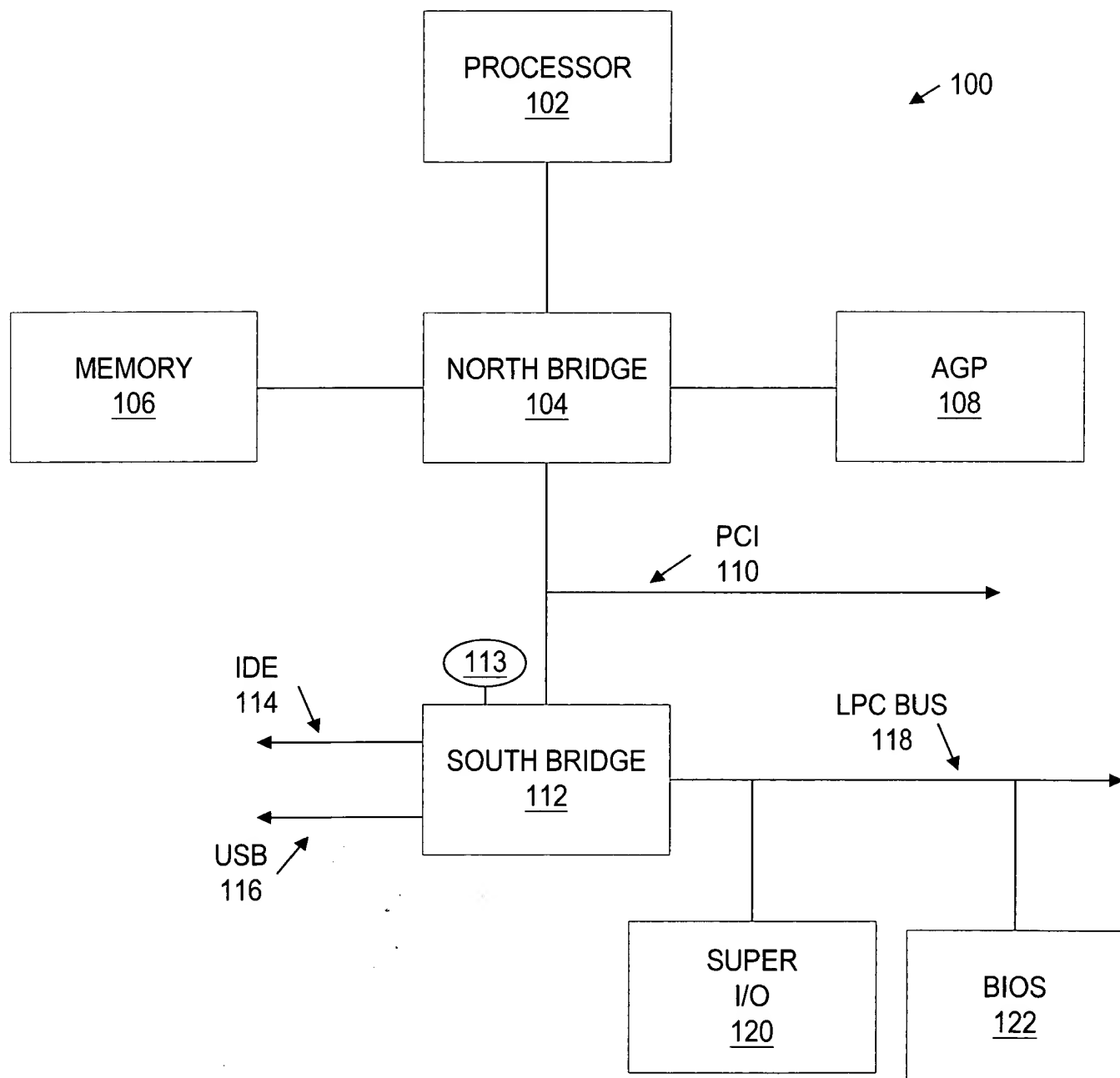
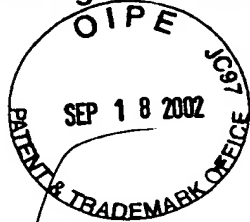


Fig. 1A
(Prior Art)



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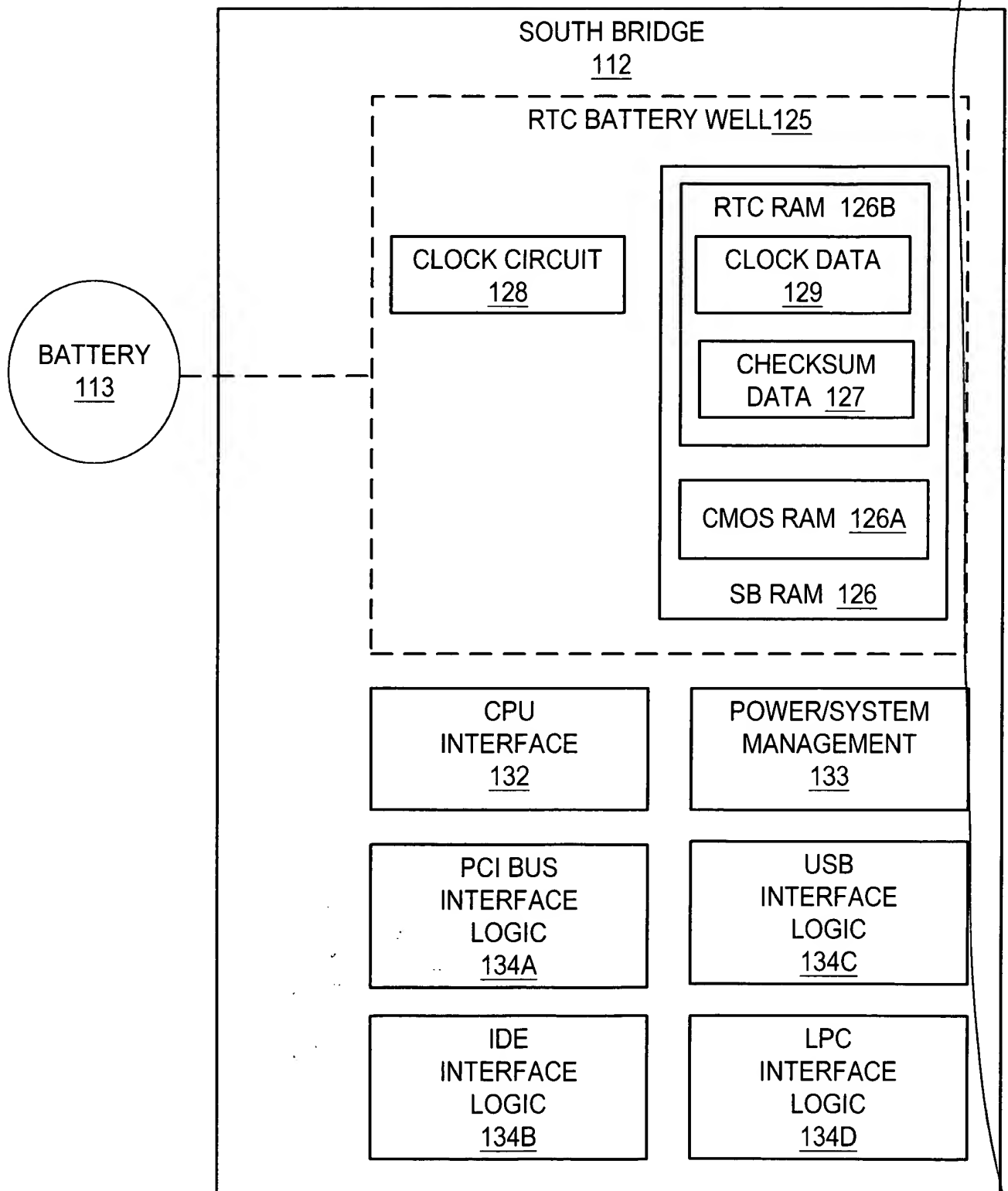


Fig. 1B
(Prior Art)

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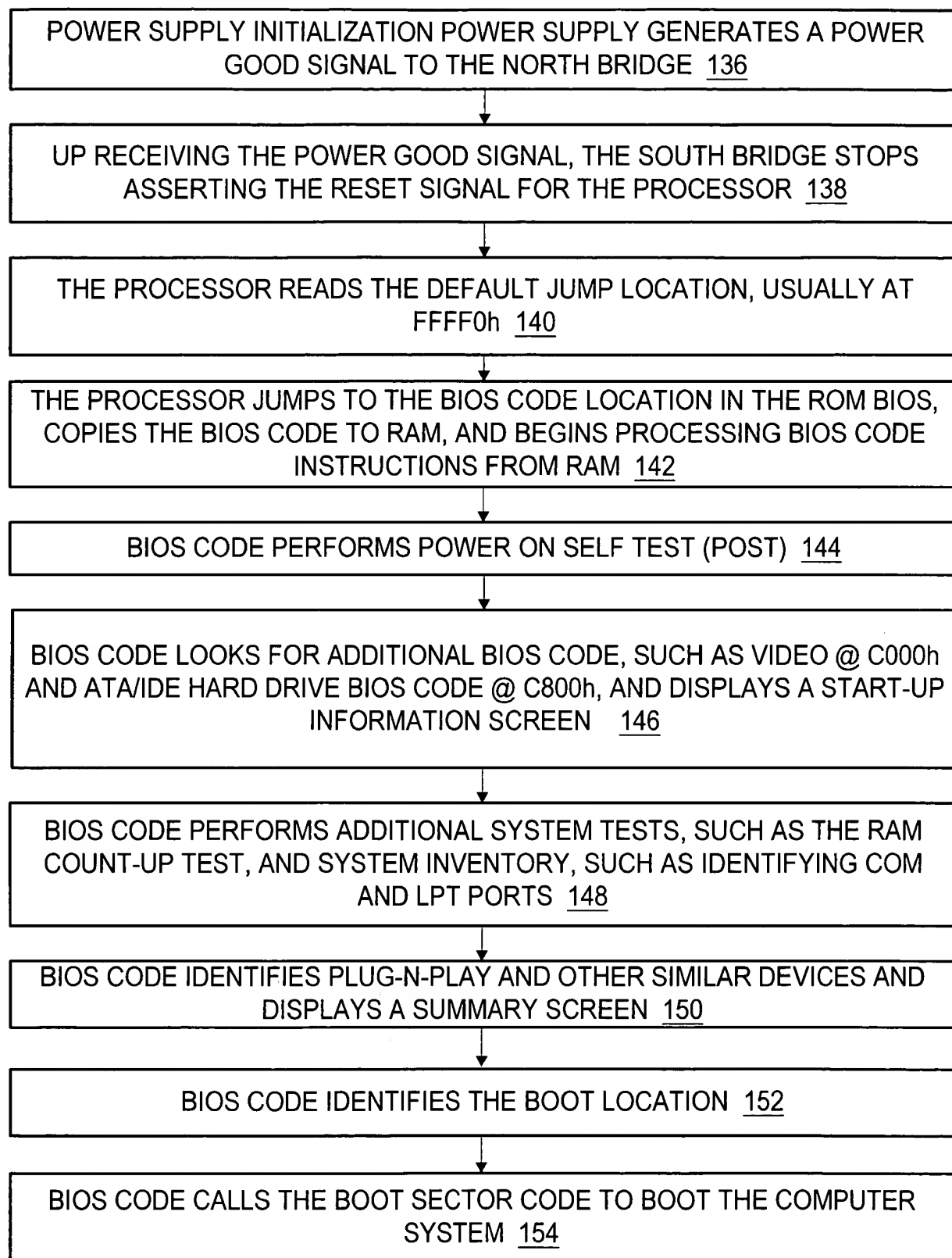


Fig. 2A
(Prior Art)

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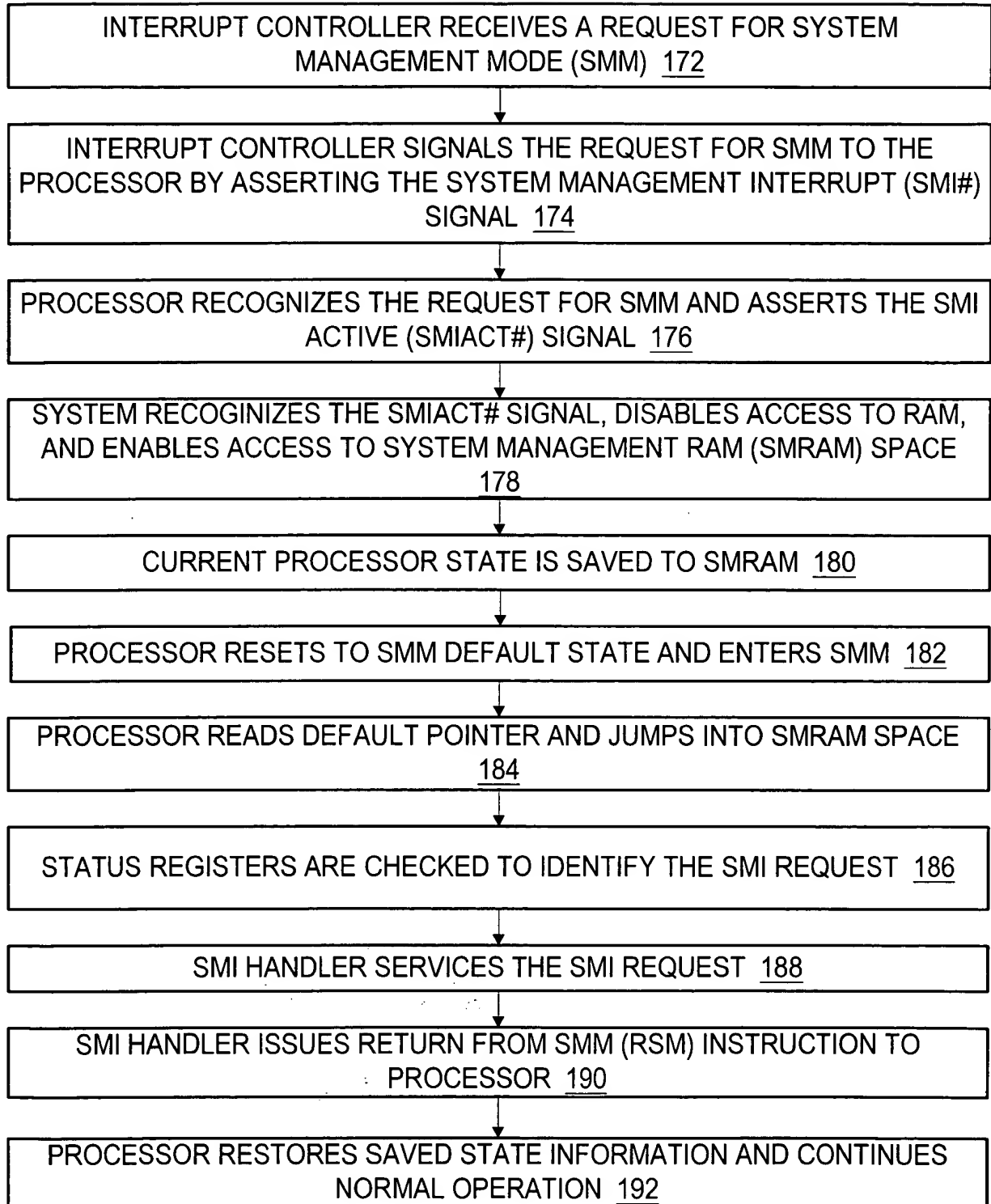


Fig. 2B
(Prior Art)

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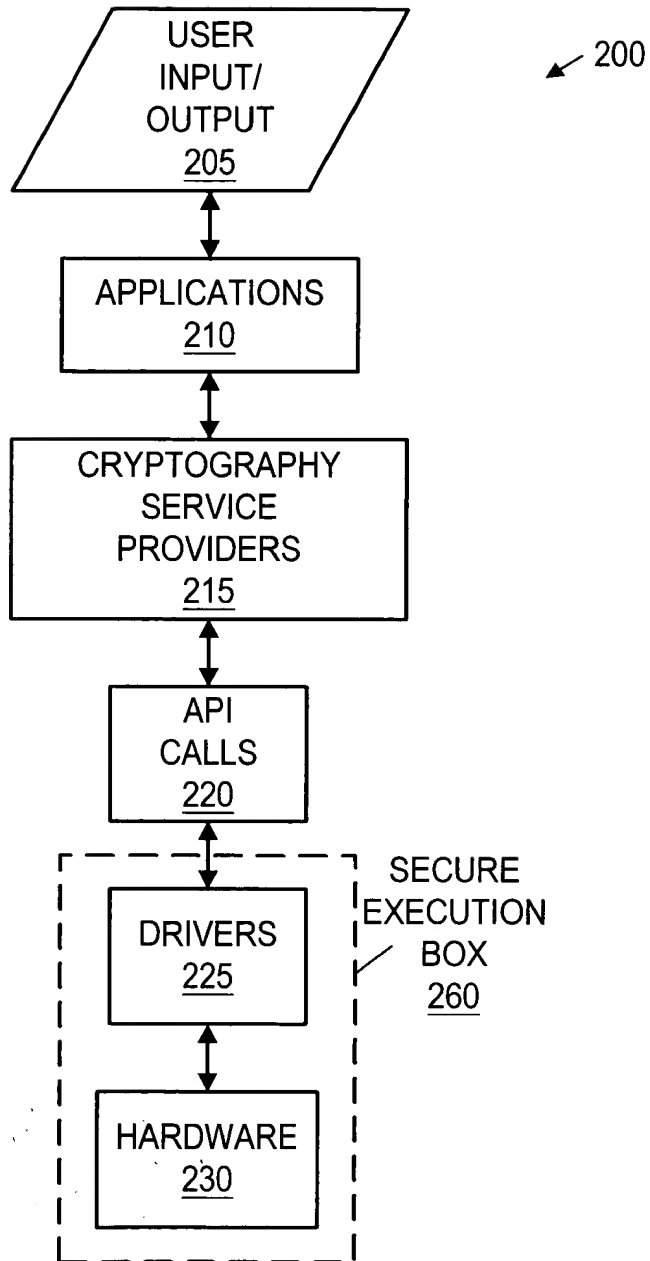
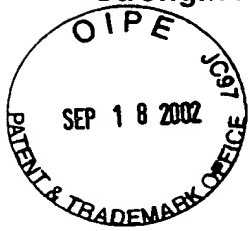
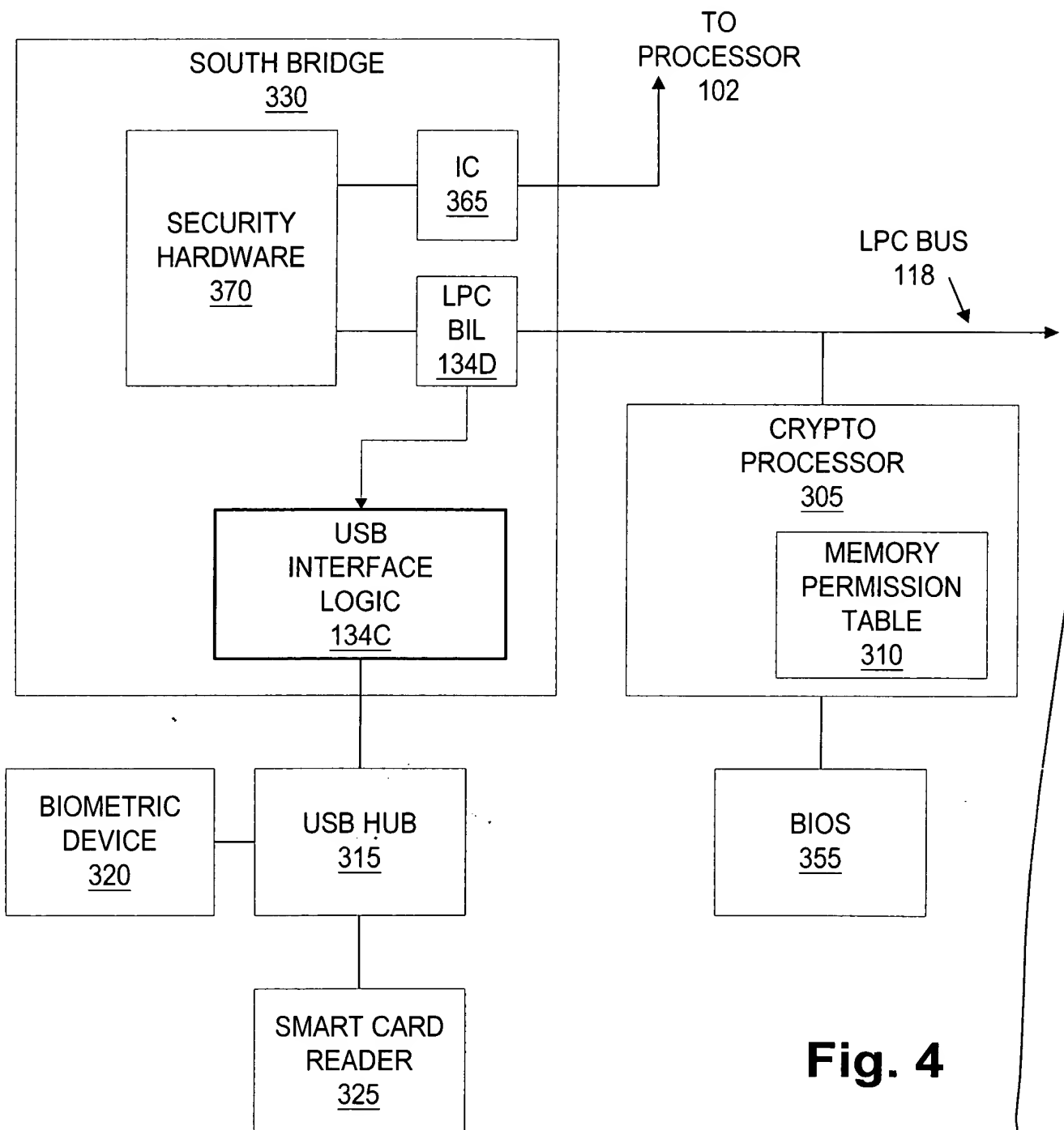


Fig. [3] 2

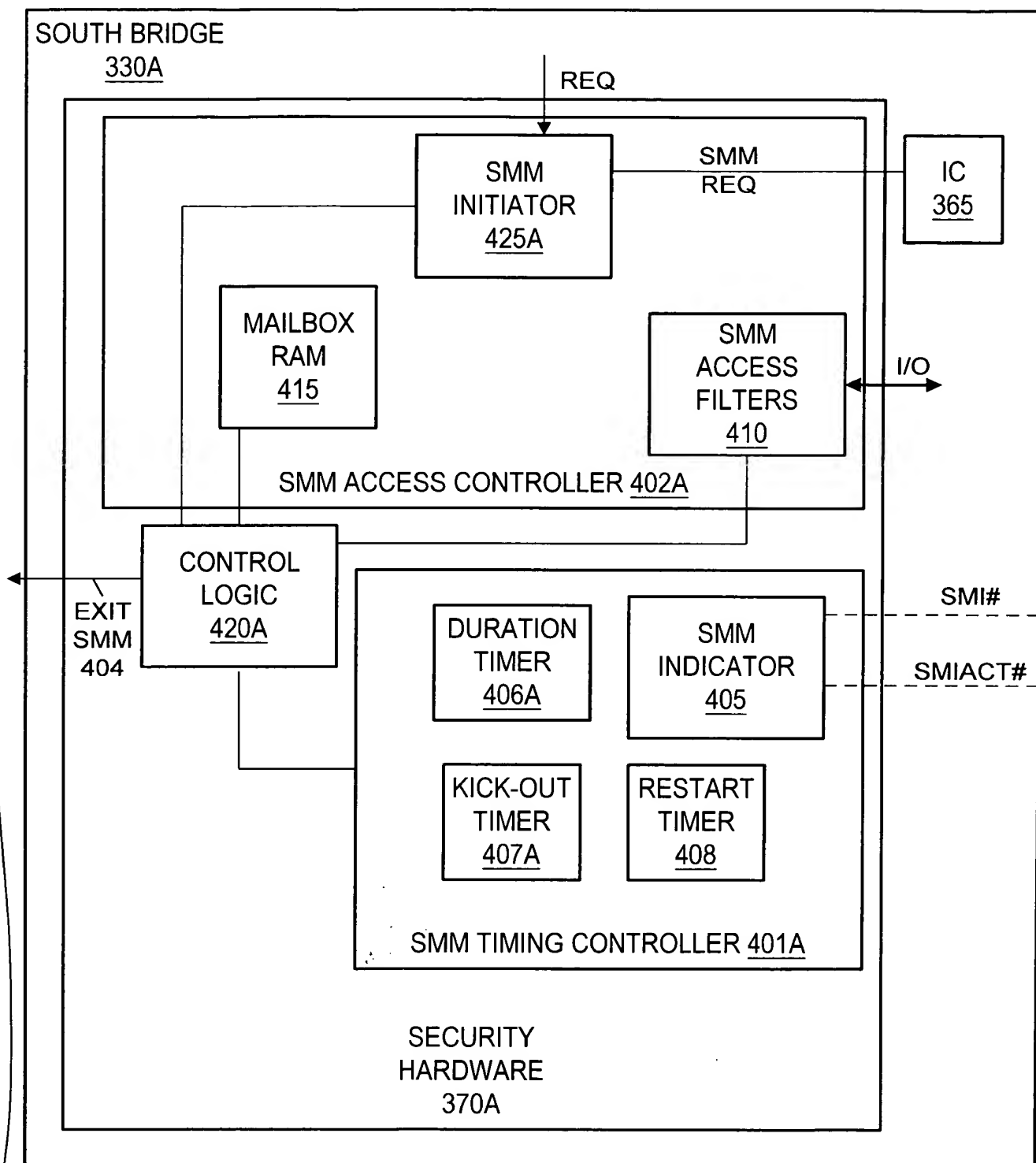


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**Fig. 4**



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**Fig. 5A**



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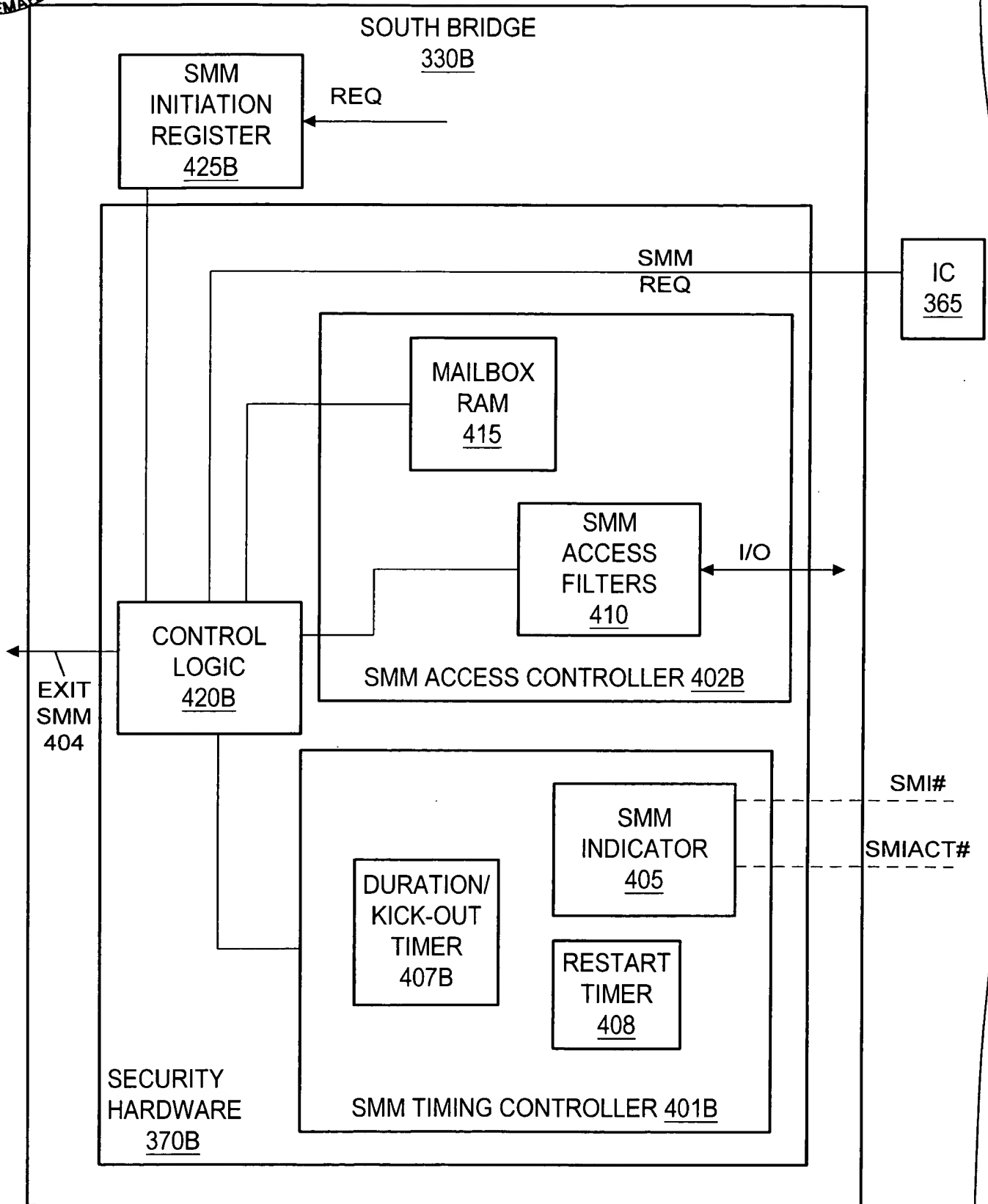


Fig. 5B

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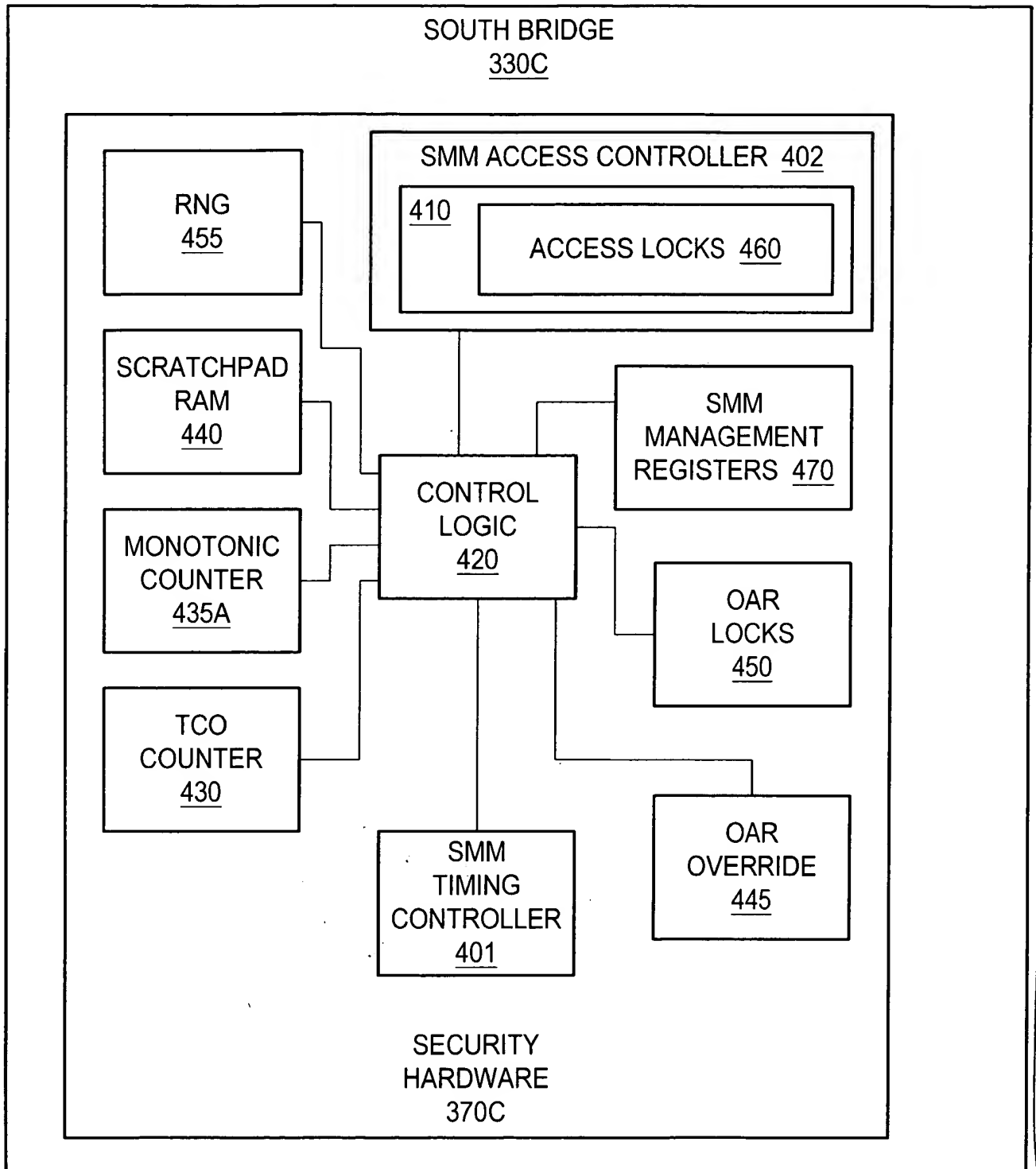


Fig. 6



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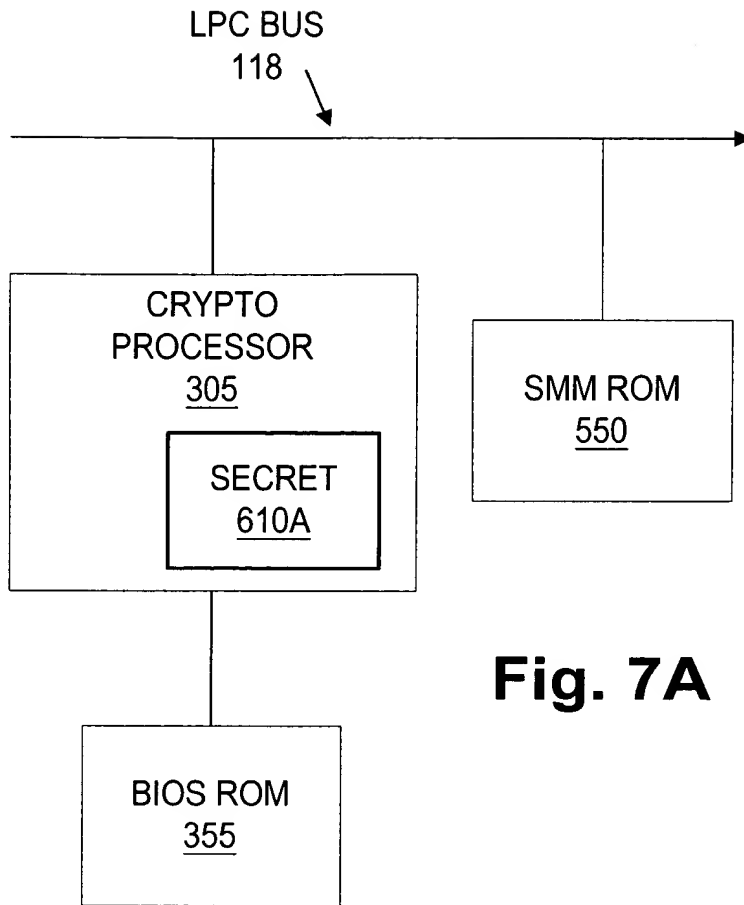


Fig. 7A

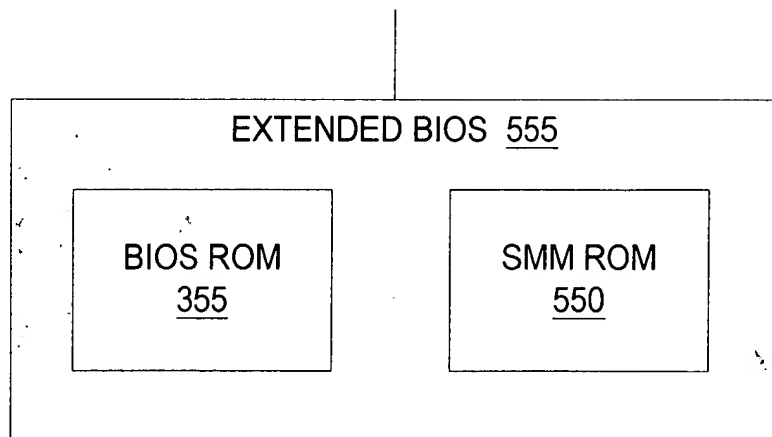


Fig. 7B



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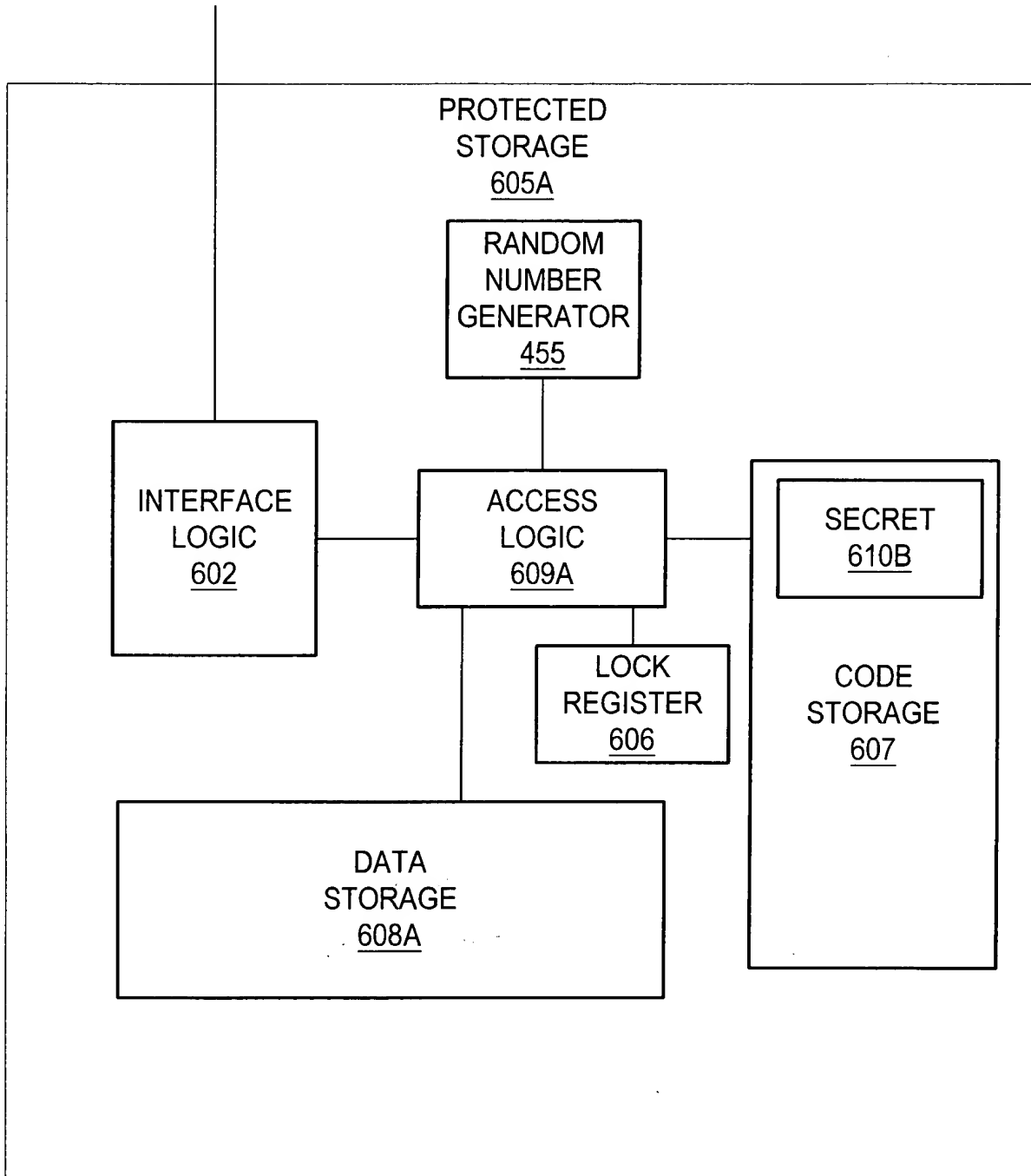


Fig. 7C



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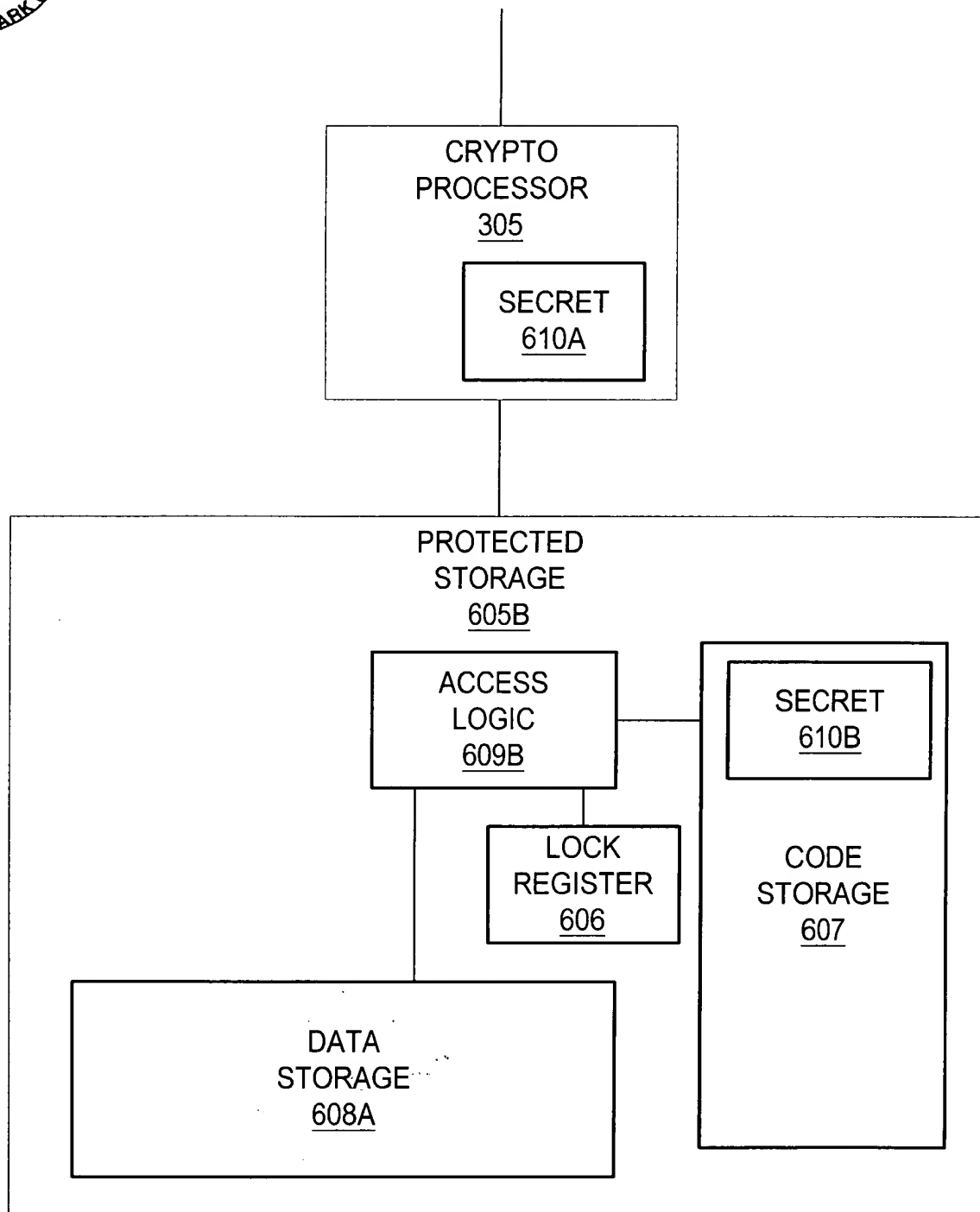


Fig. 7D



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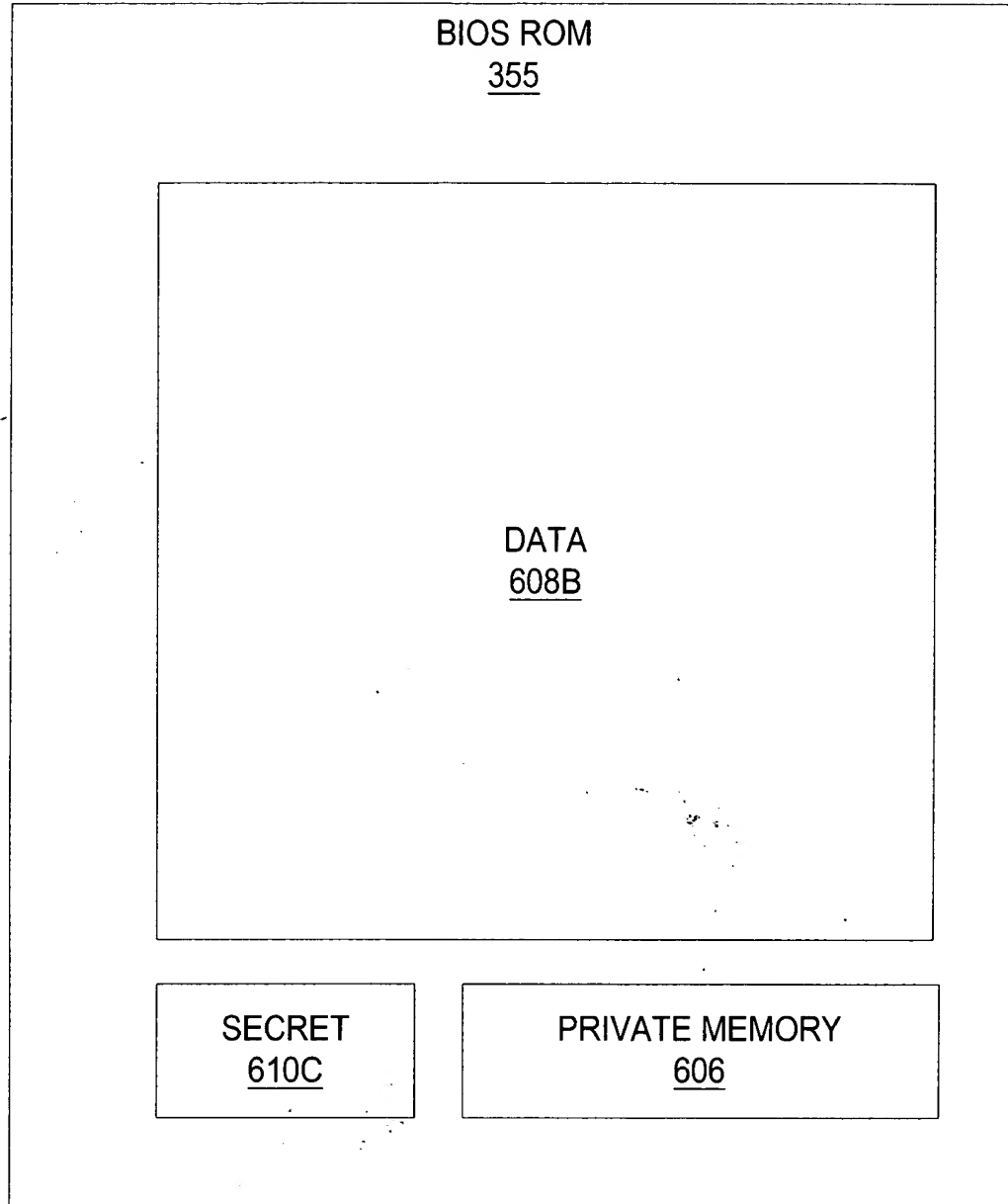


Fig. 8A

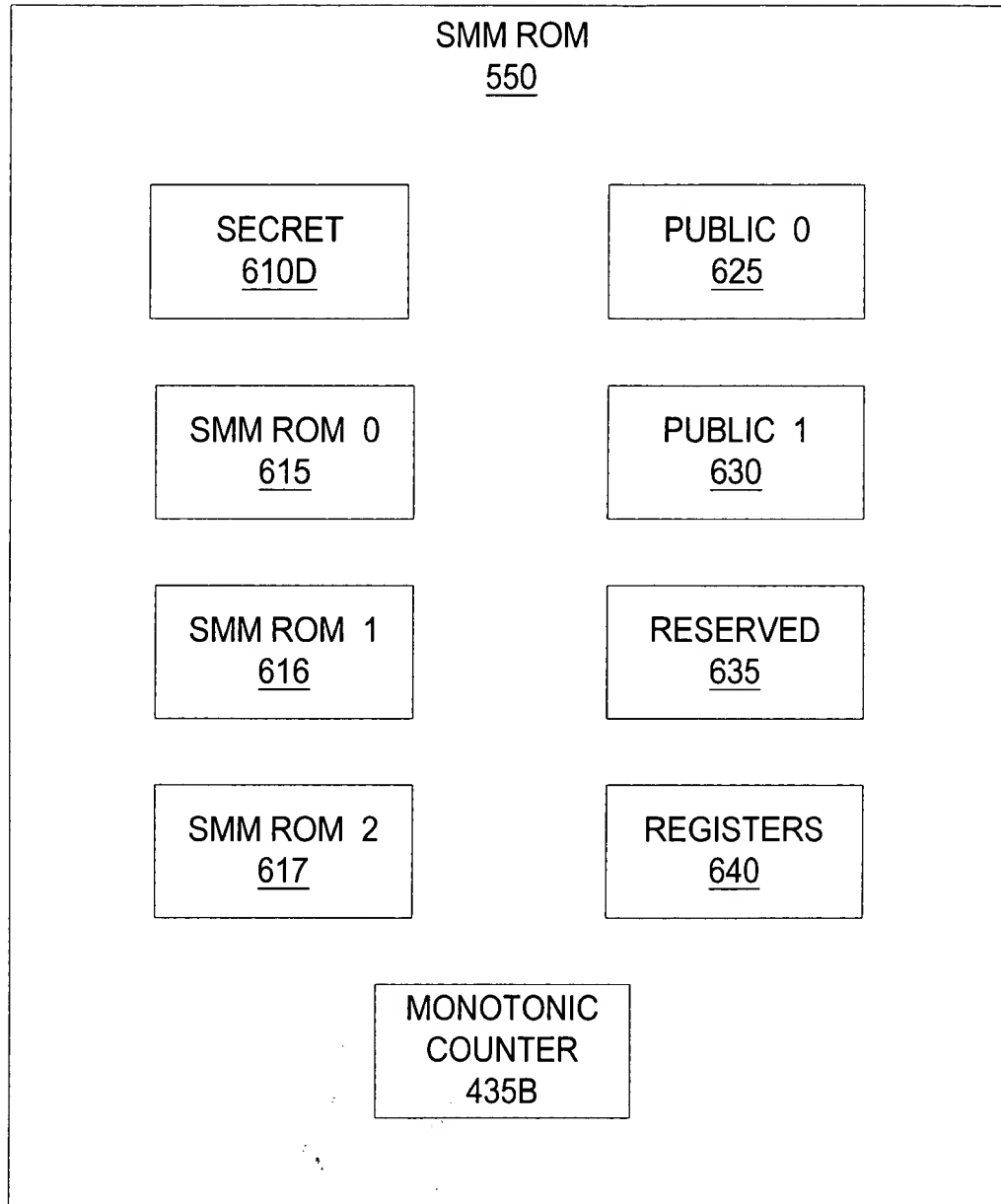
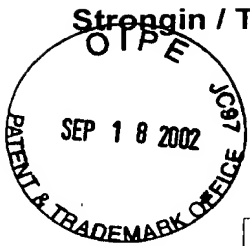


Fig. 8B



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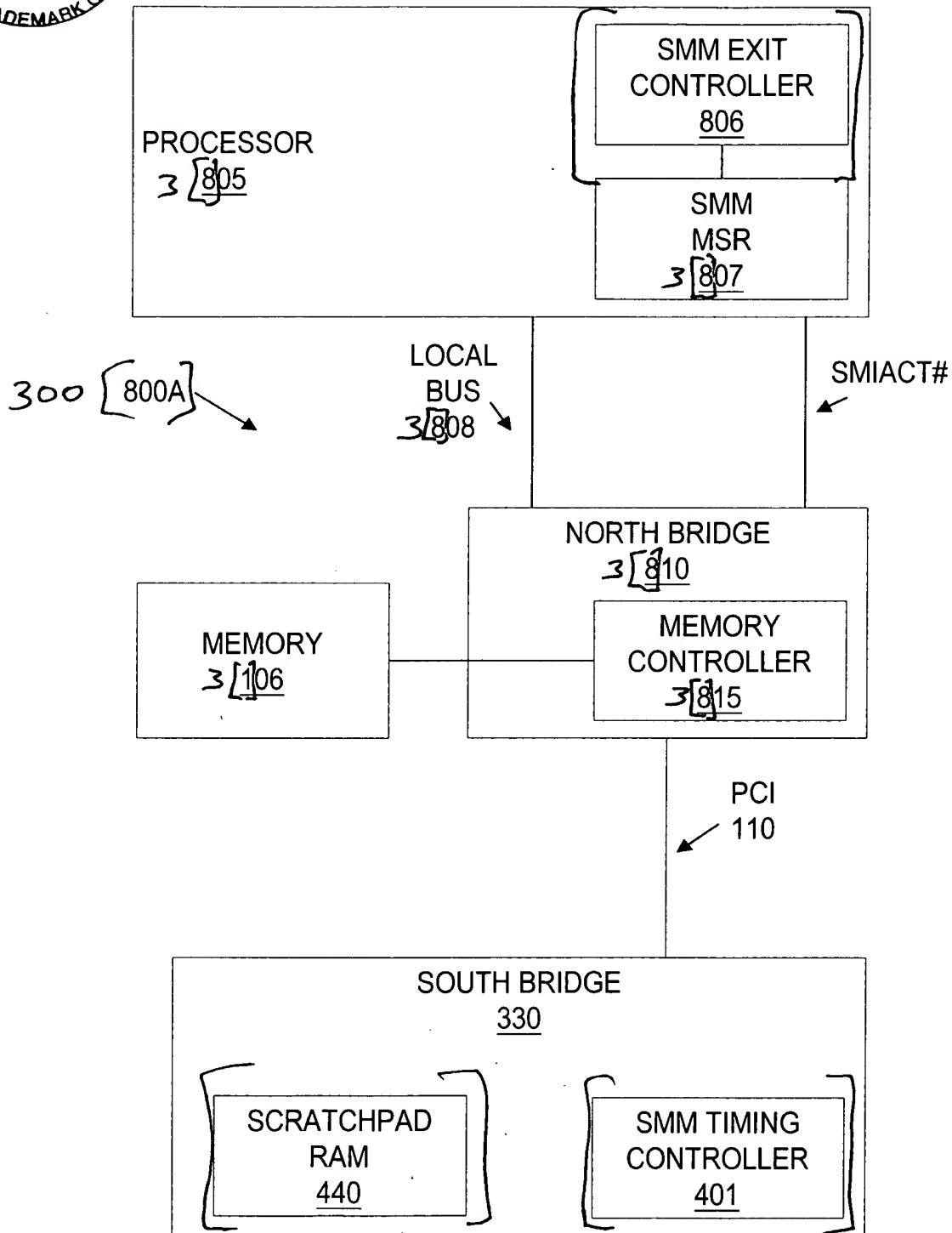


Fig. 9A 3



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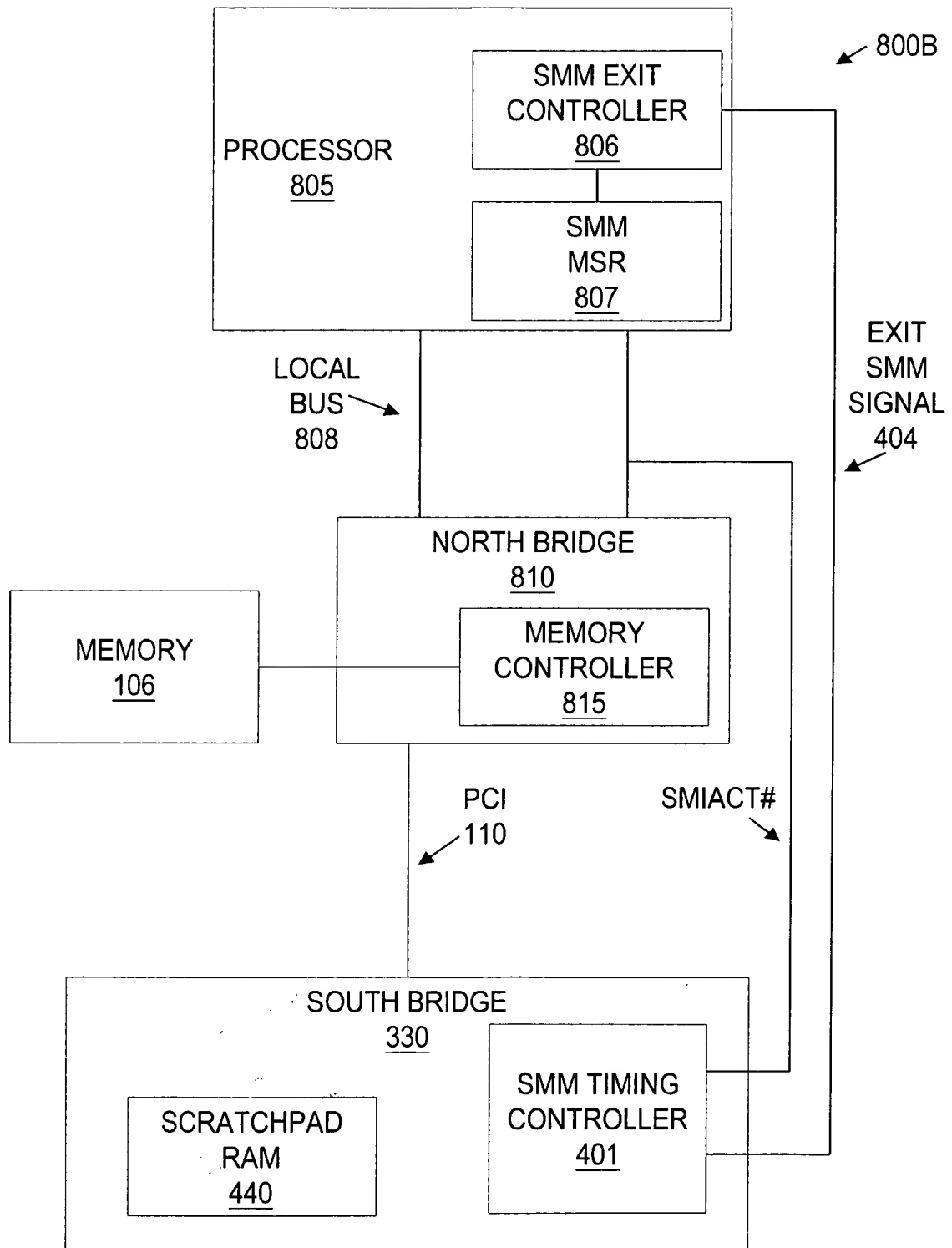


Fig. 9B



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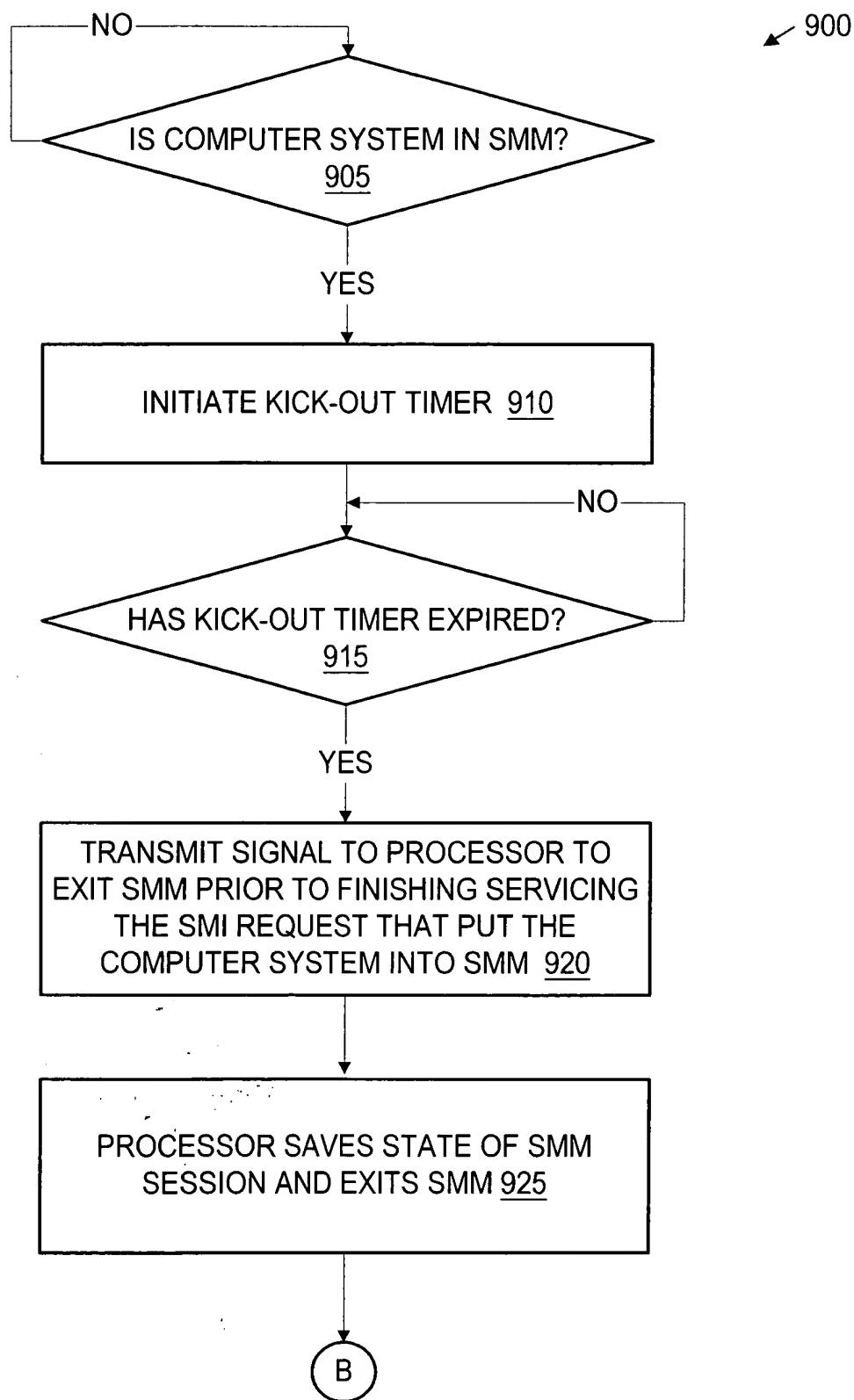


Fig. 10A

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B

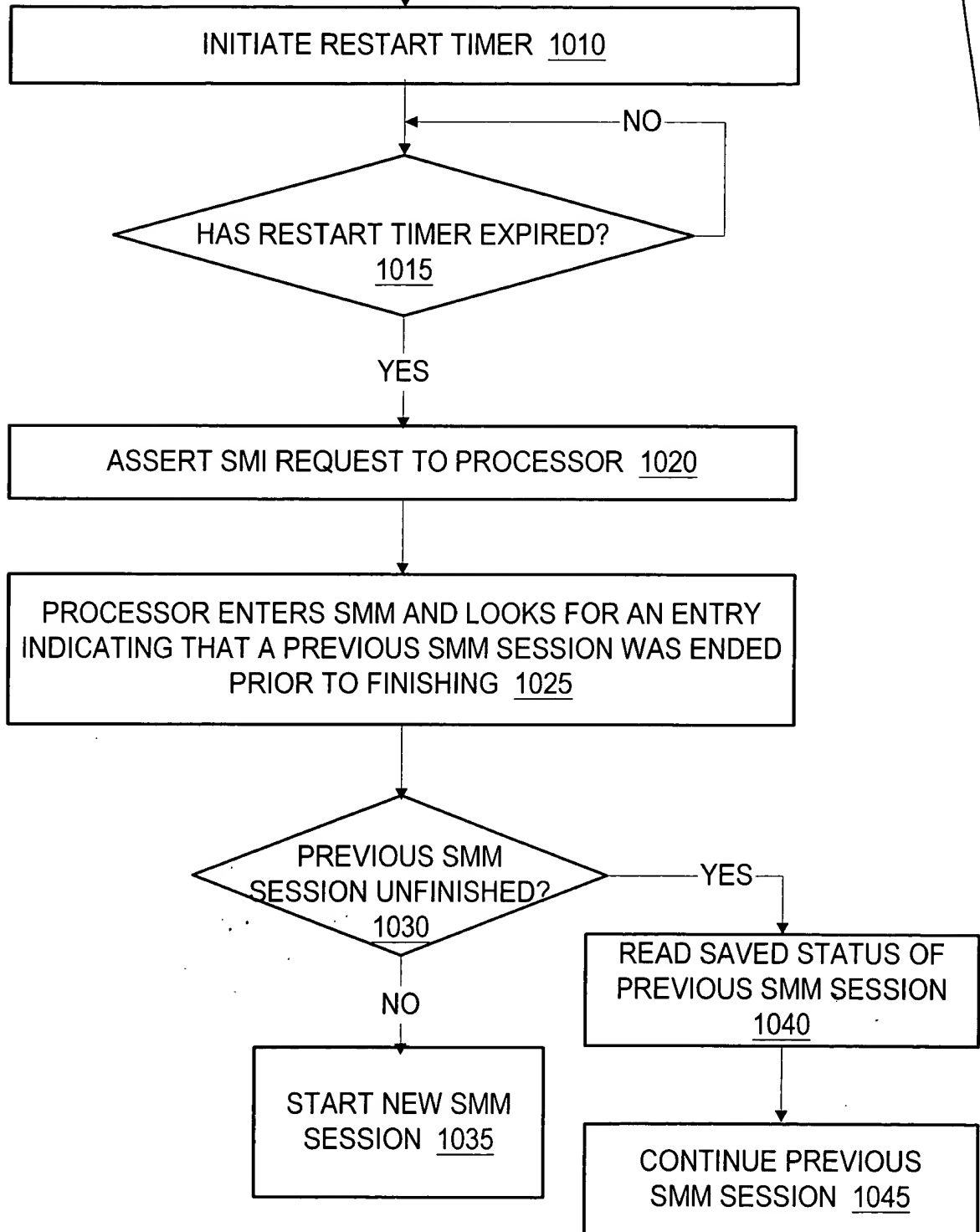


Fig. 10B

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1100A

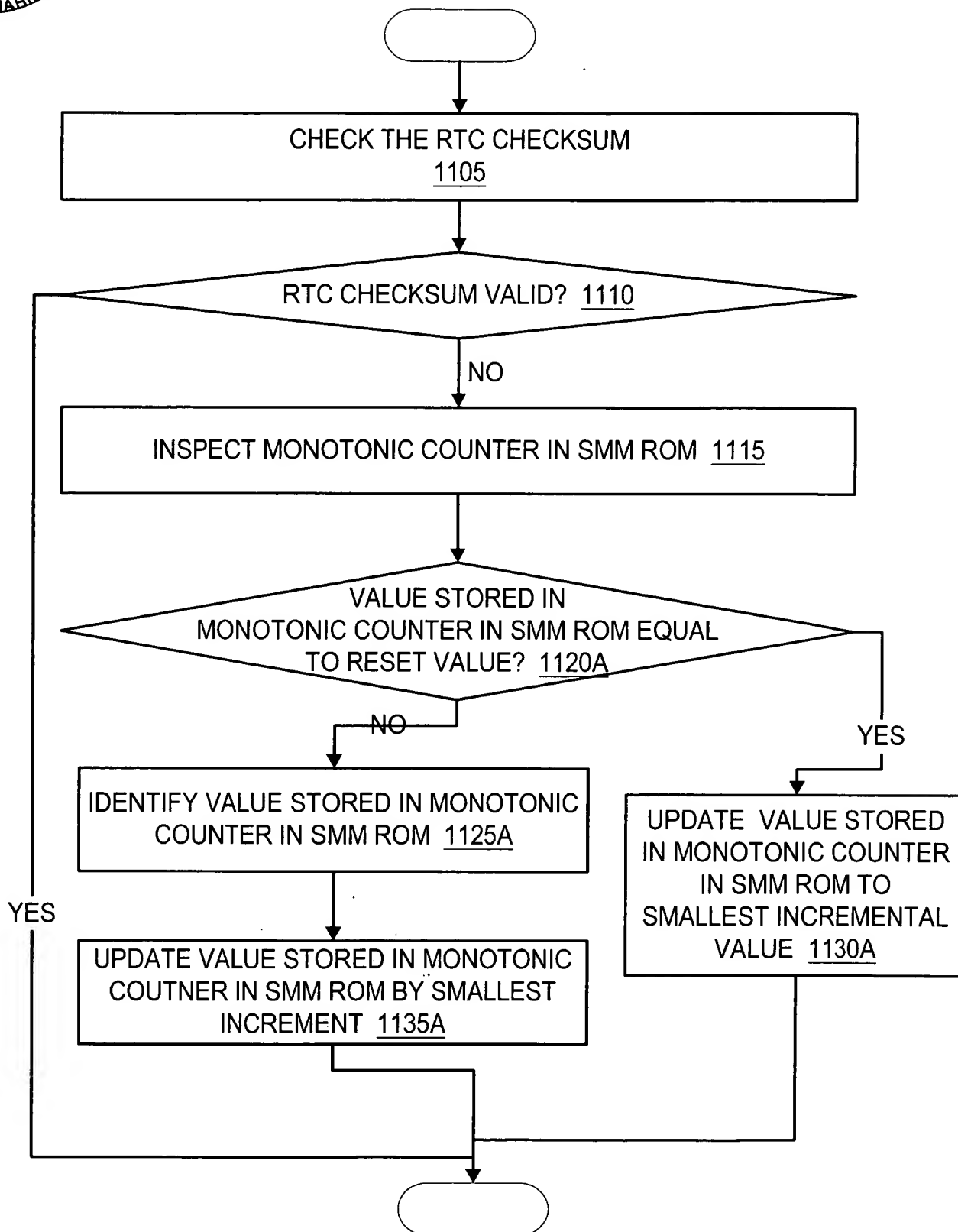


Fig. 11A



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1100B

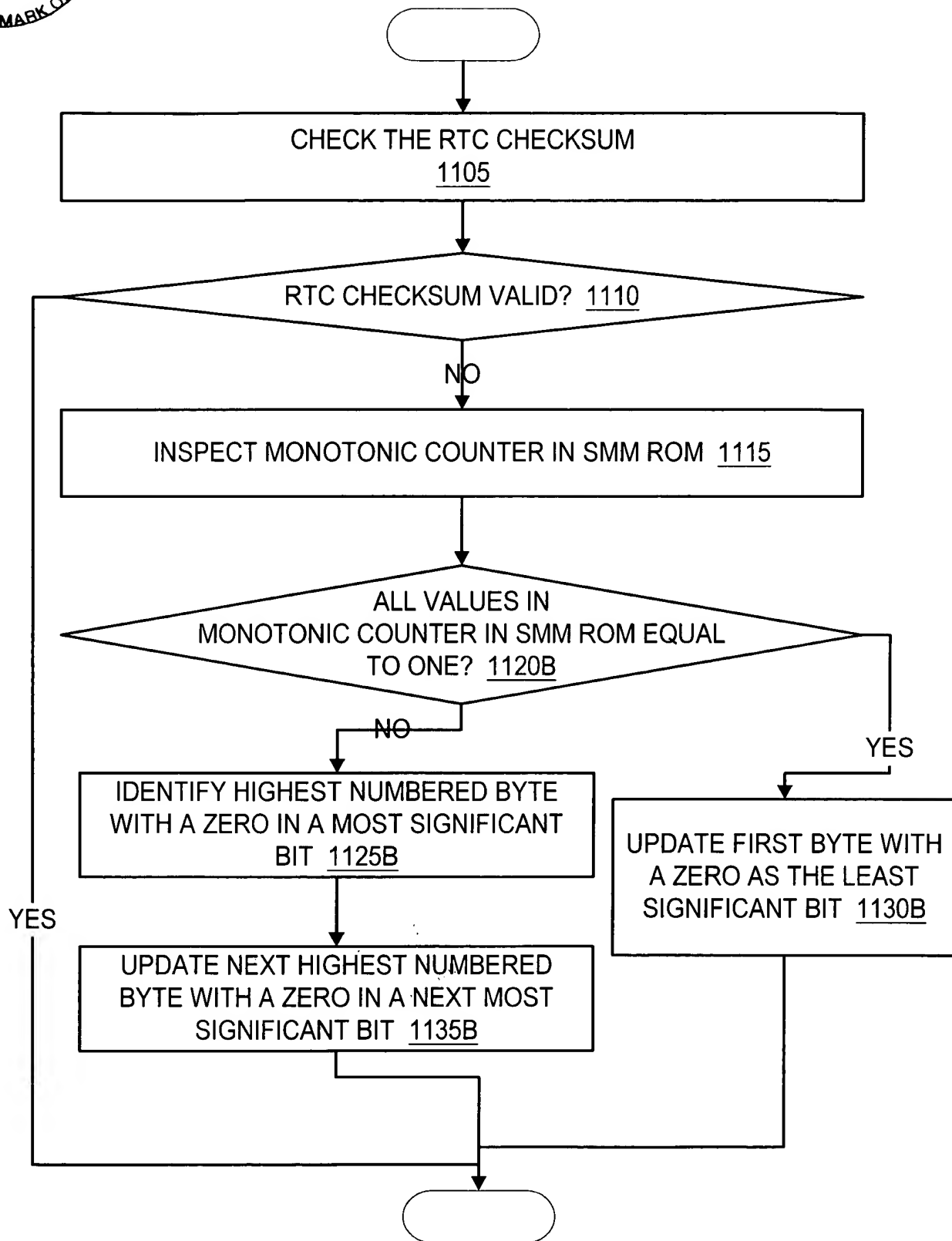


Fig. 11B

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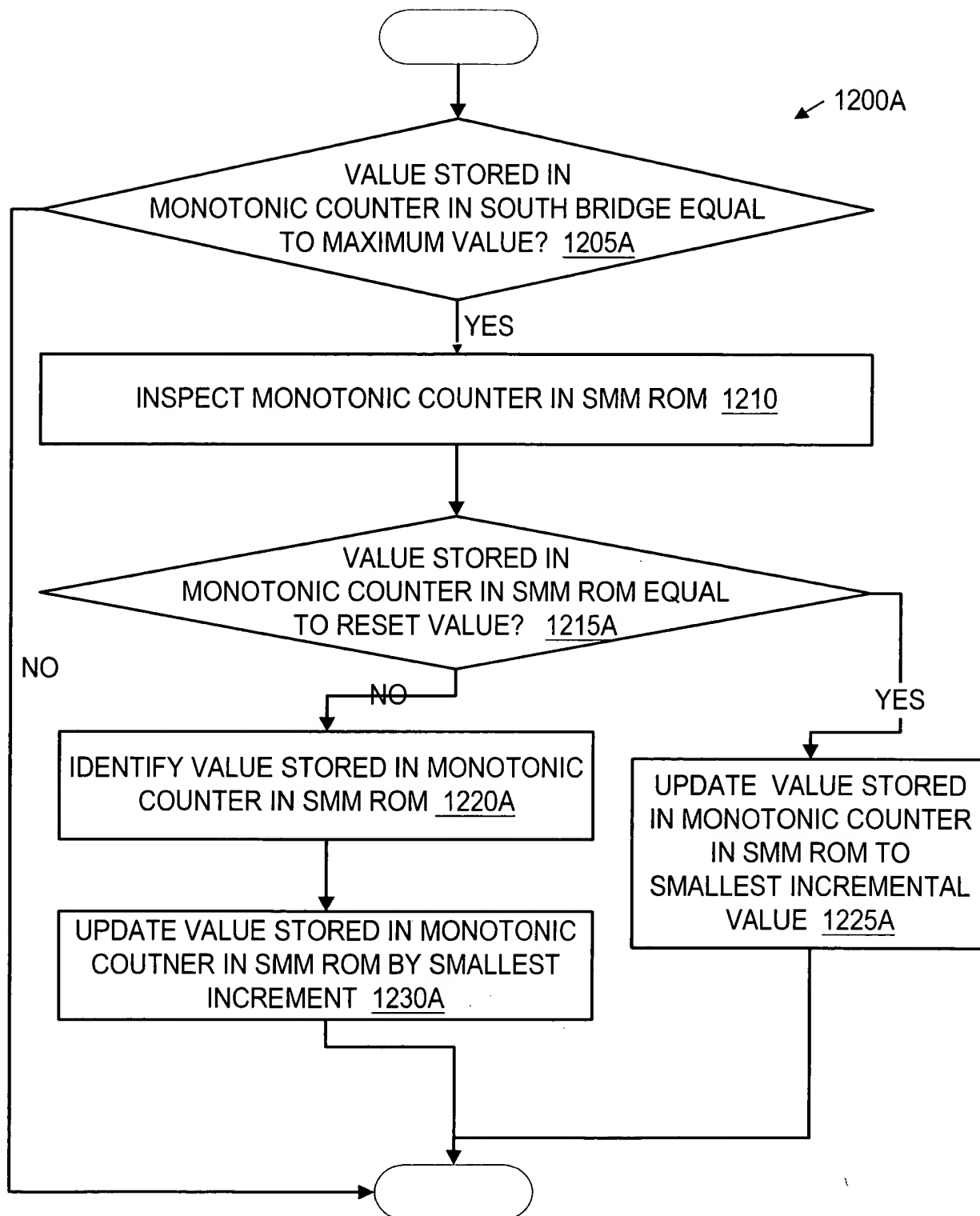


Fig. 12A

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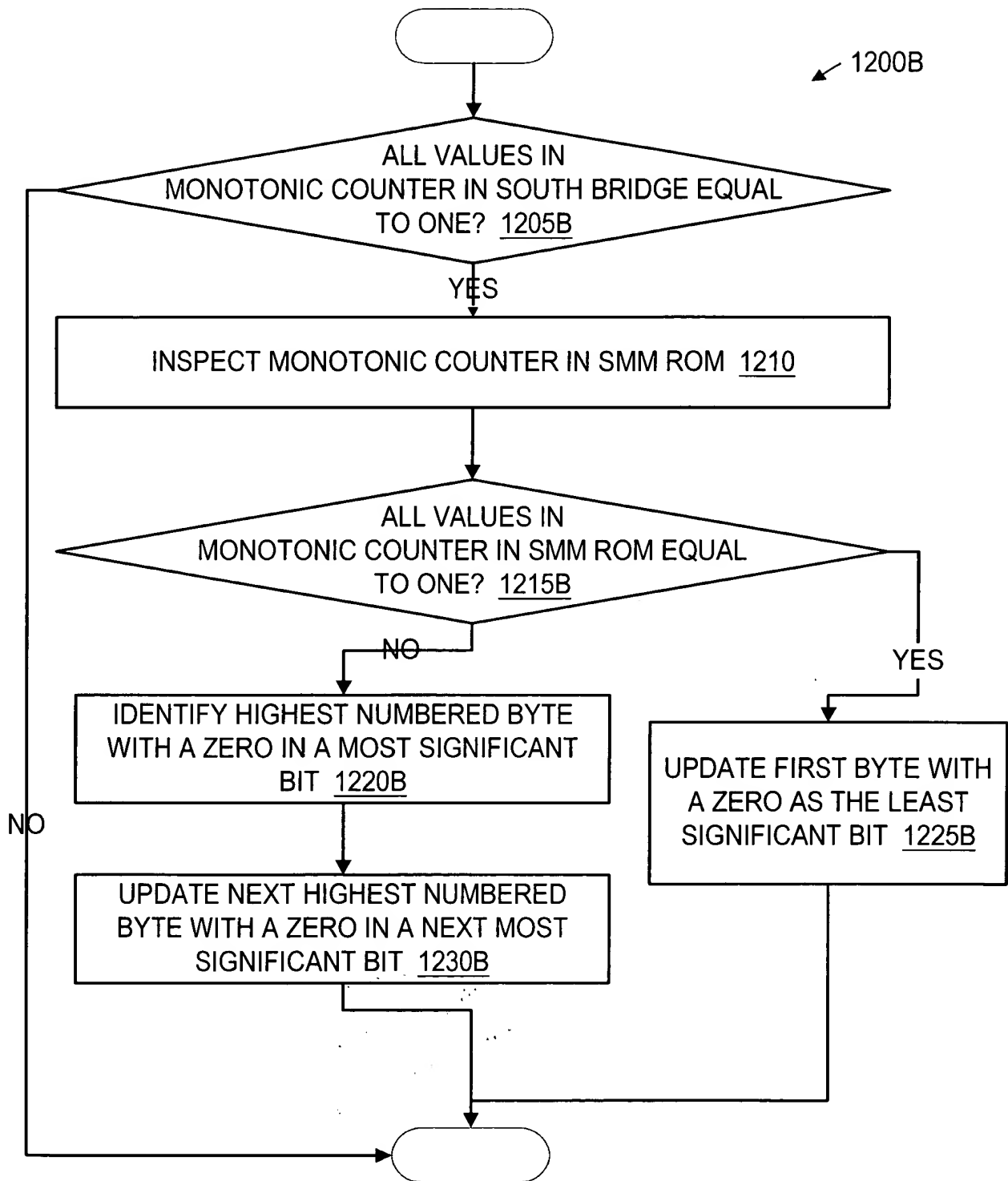


Fig. 12B



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1300A

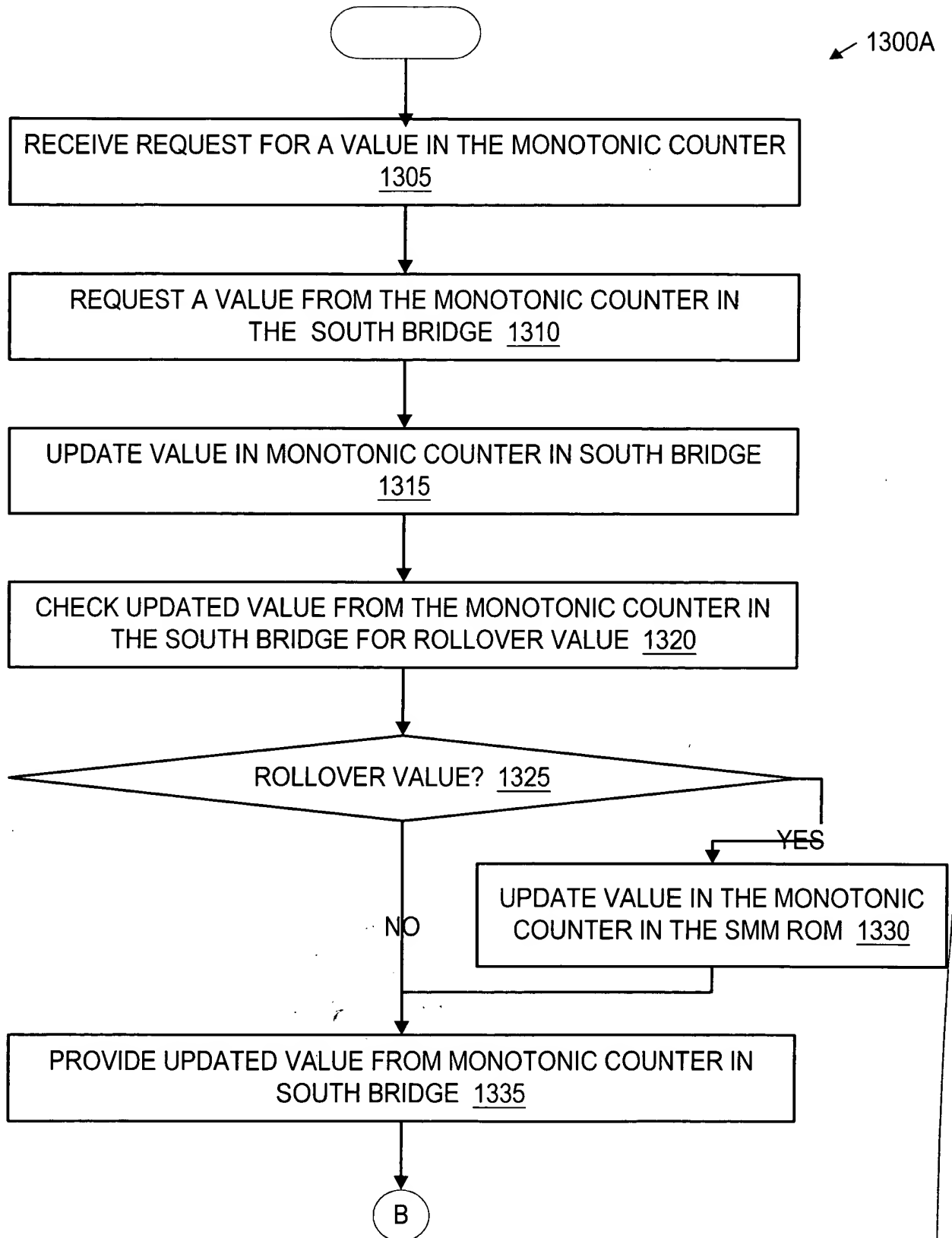
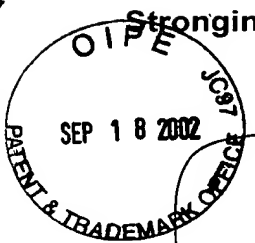


Fig. 13A



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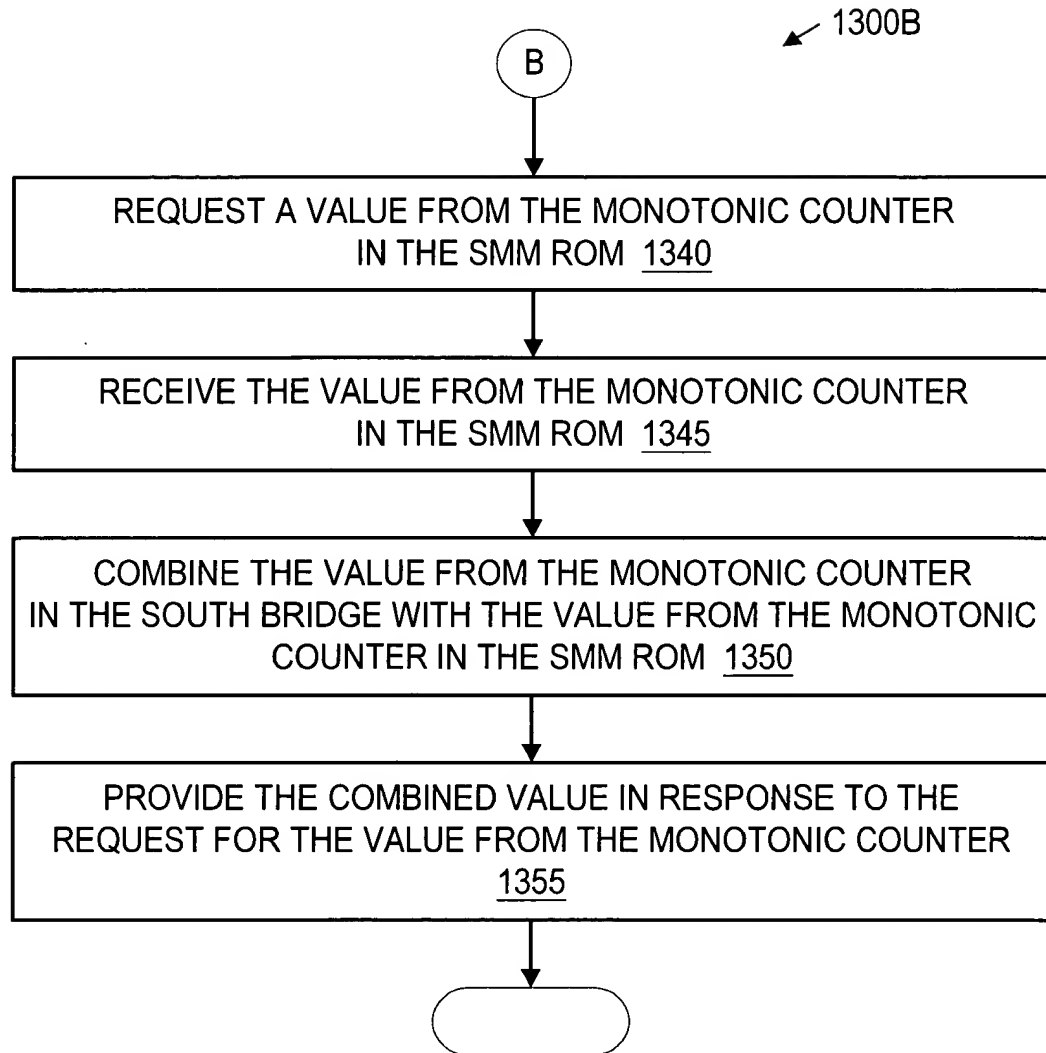


Fig. 13B

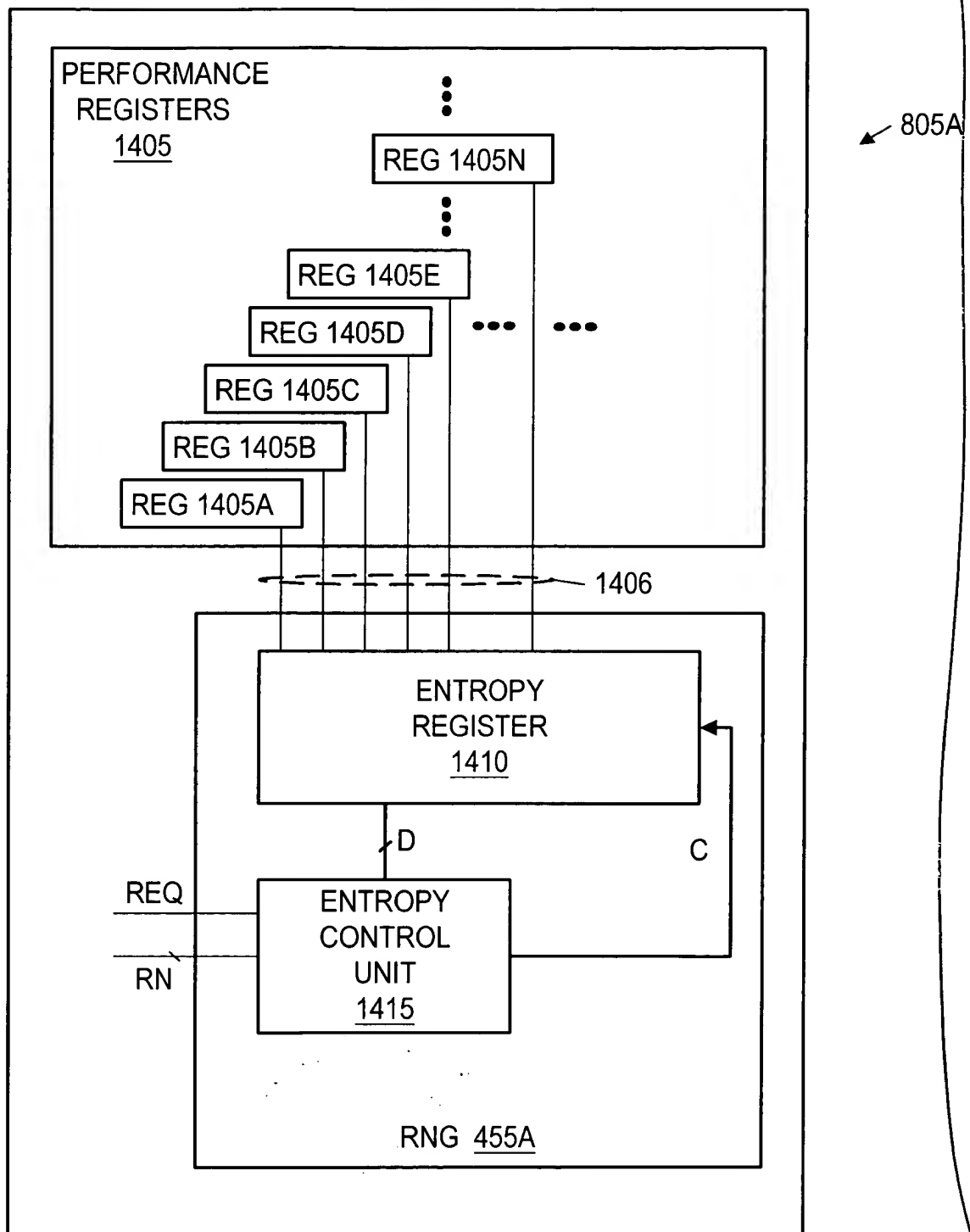


Fig. 14A

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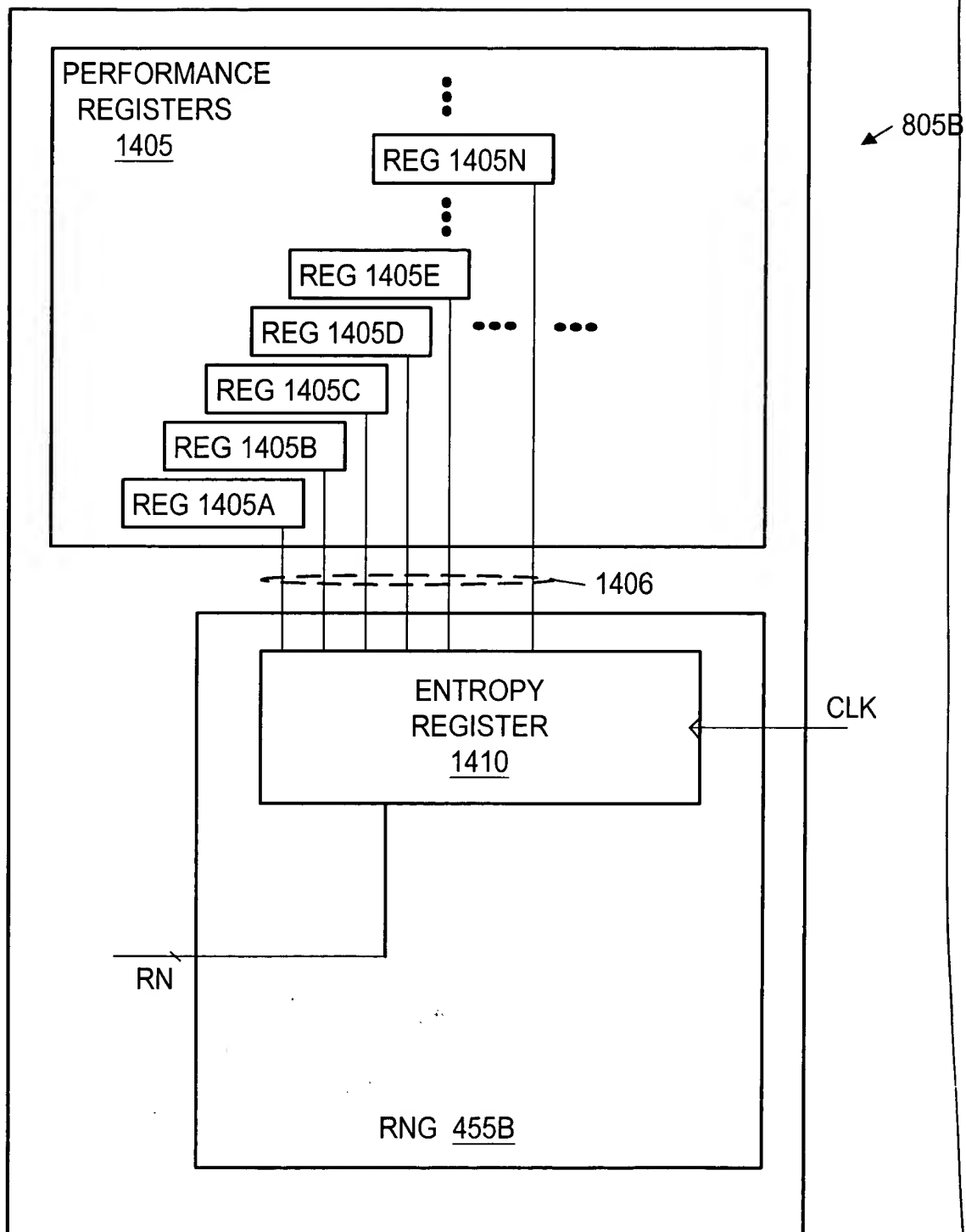
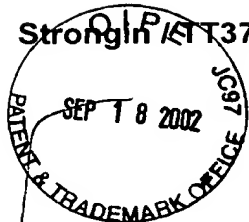


Fig. 14B



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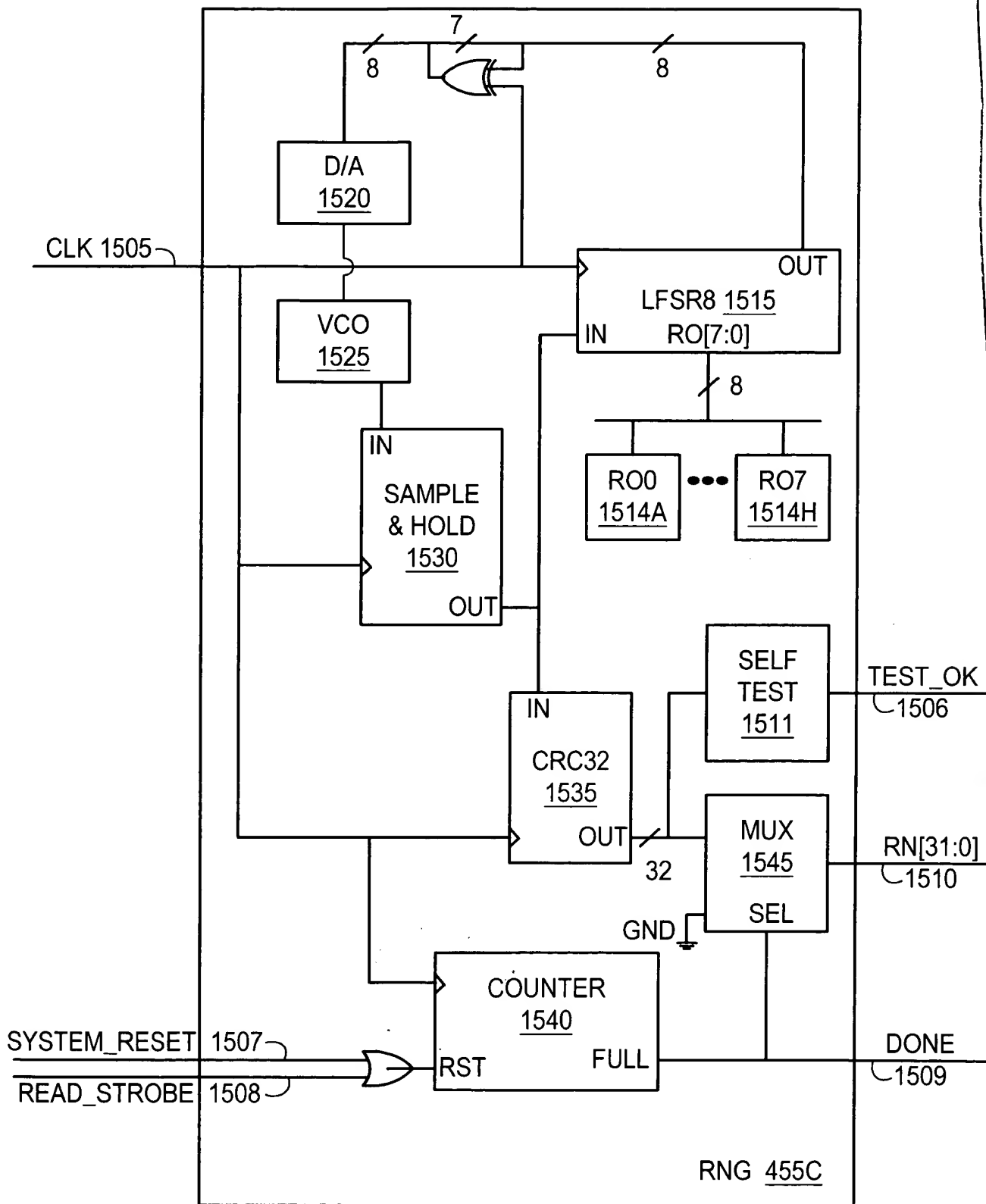


Fig. 15



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1600A

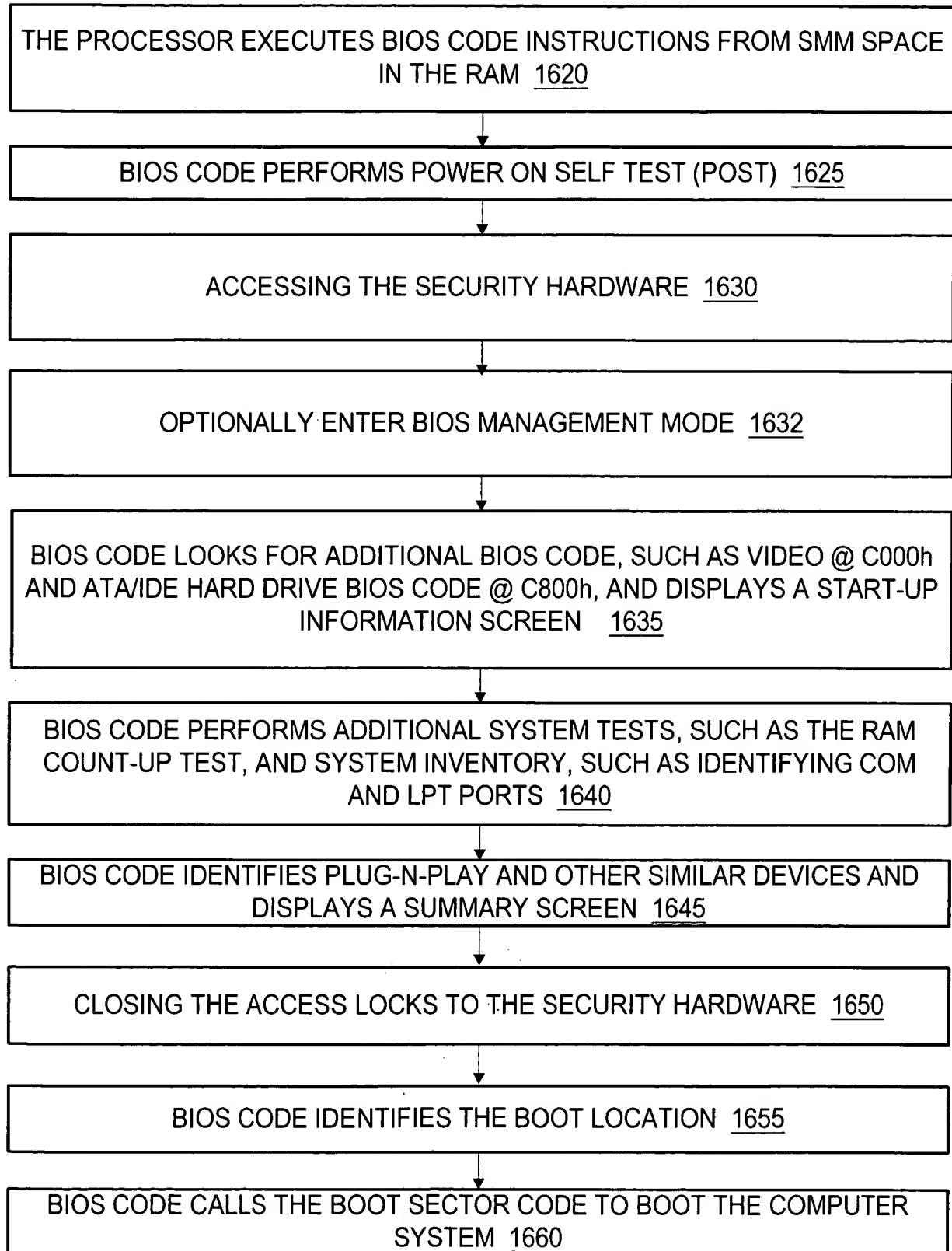


Fig. 16A



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1600B

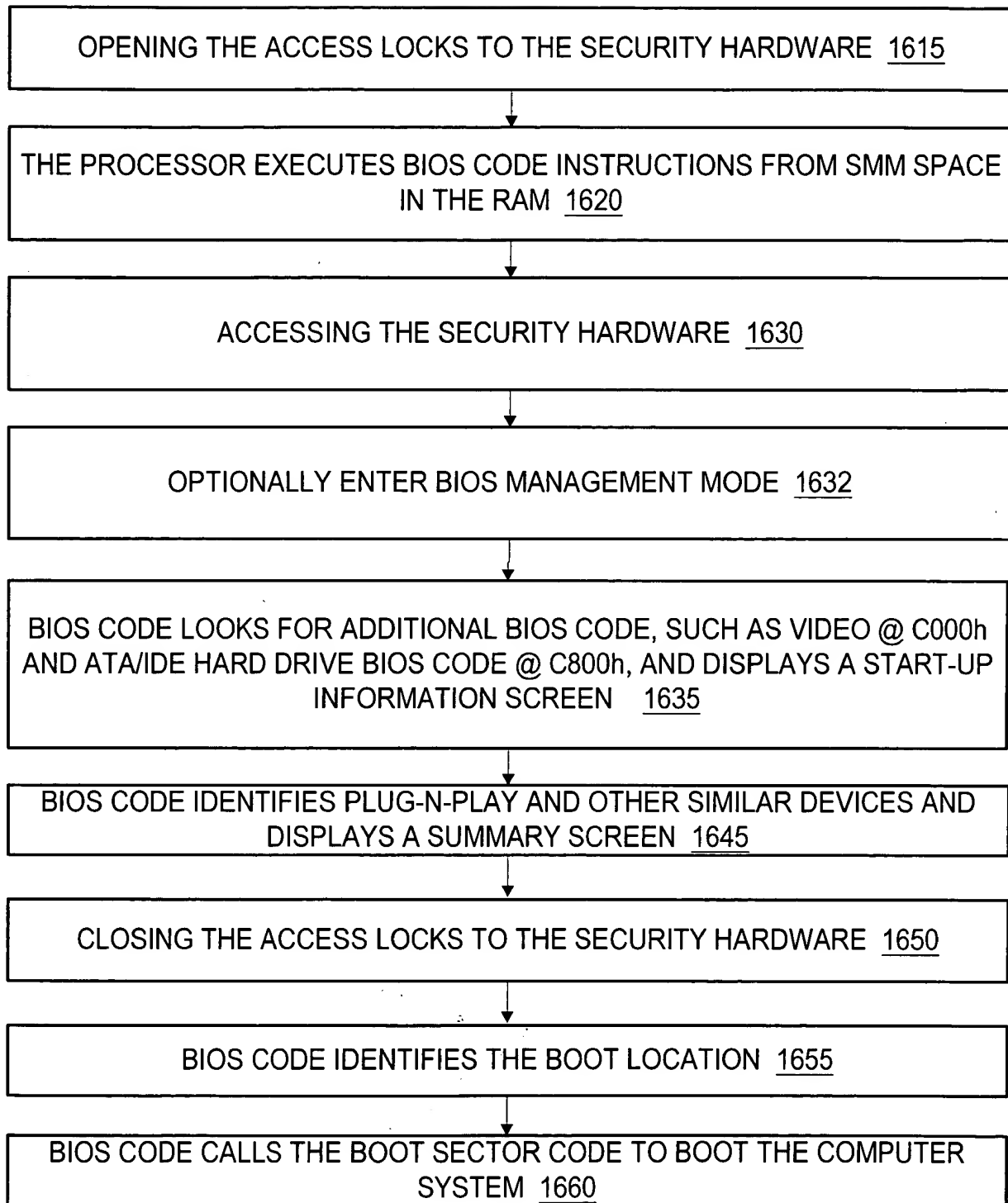


Fig. 16B



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1600C

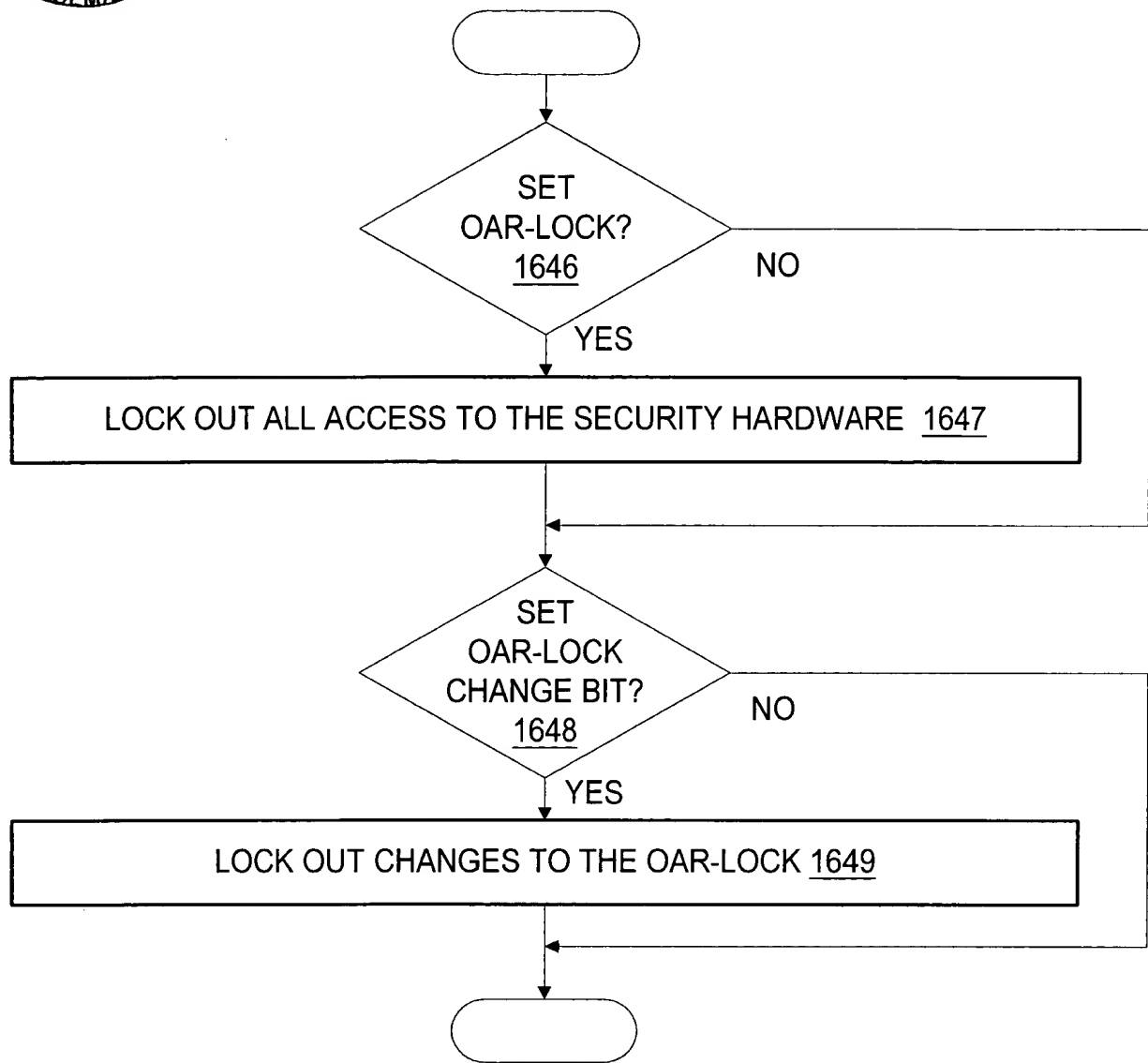
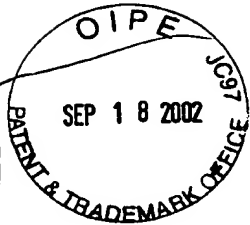


Fig. 16C



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1600D

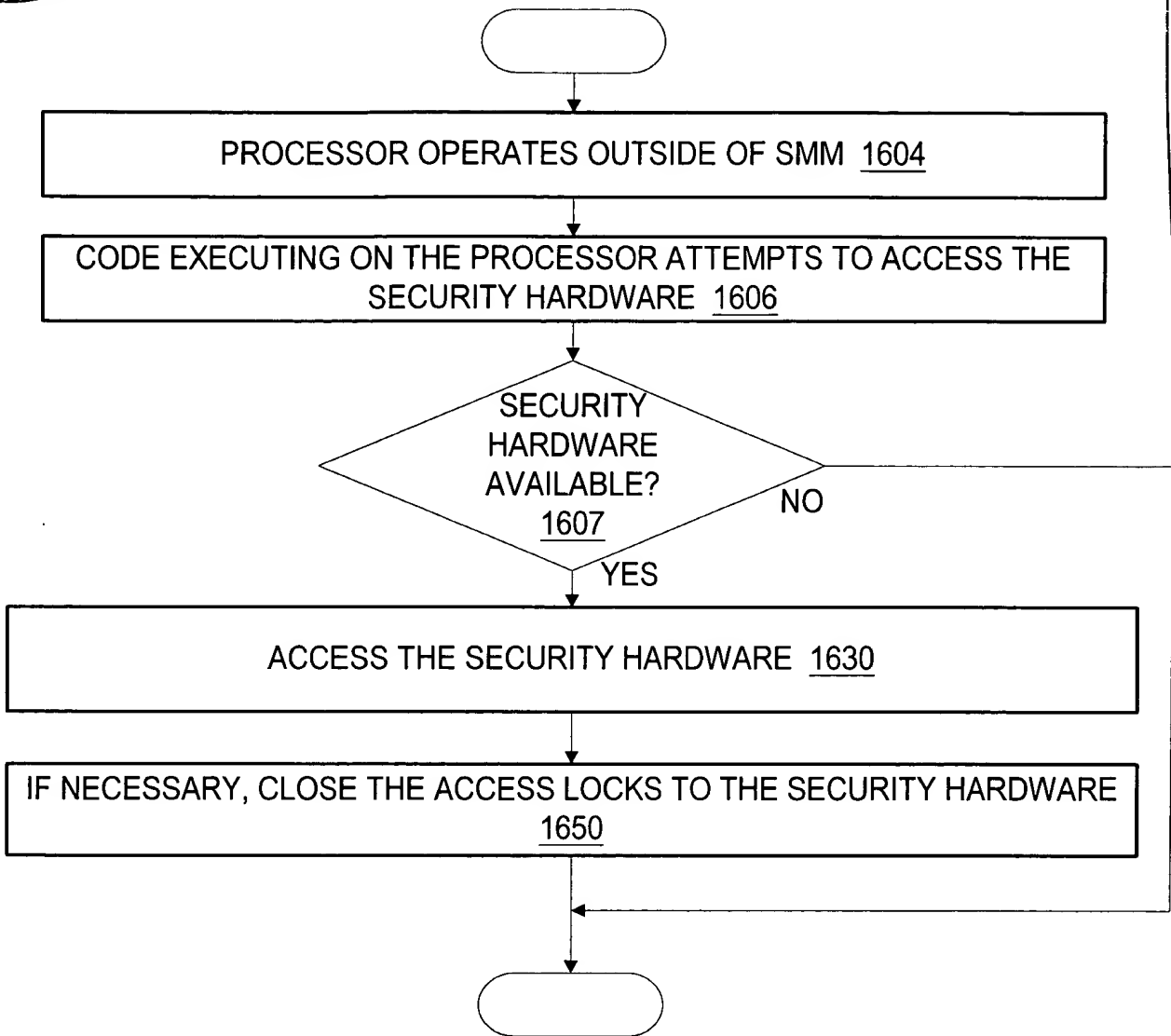
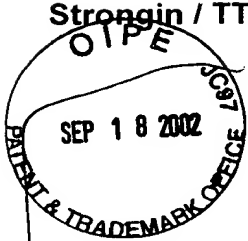


Fig. 16D



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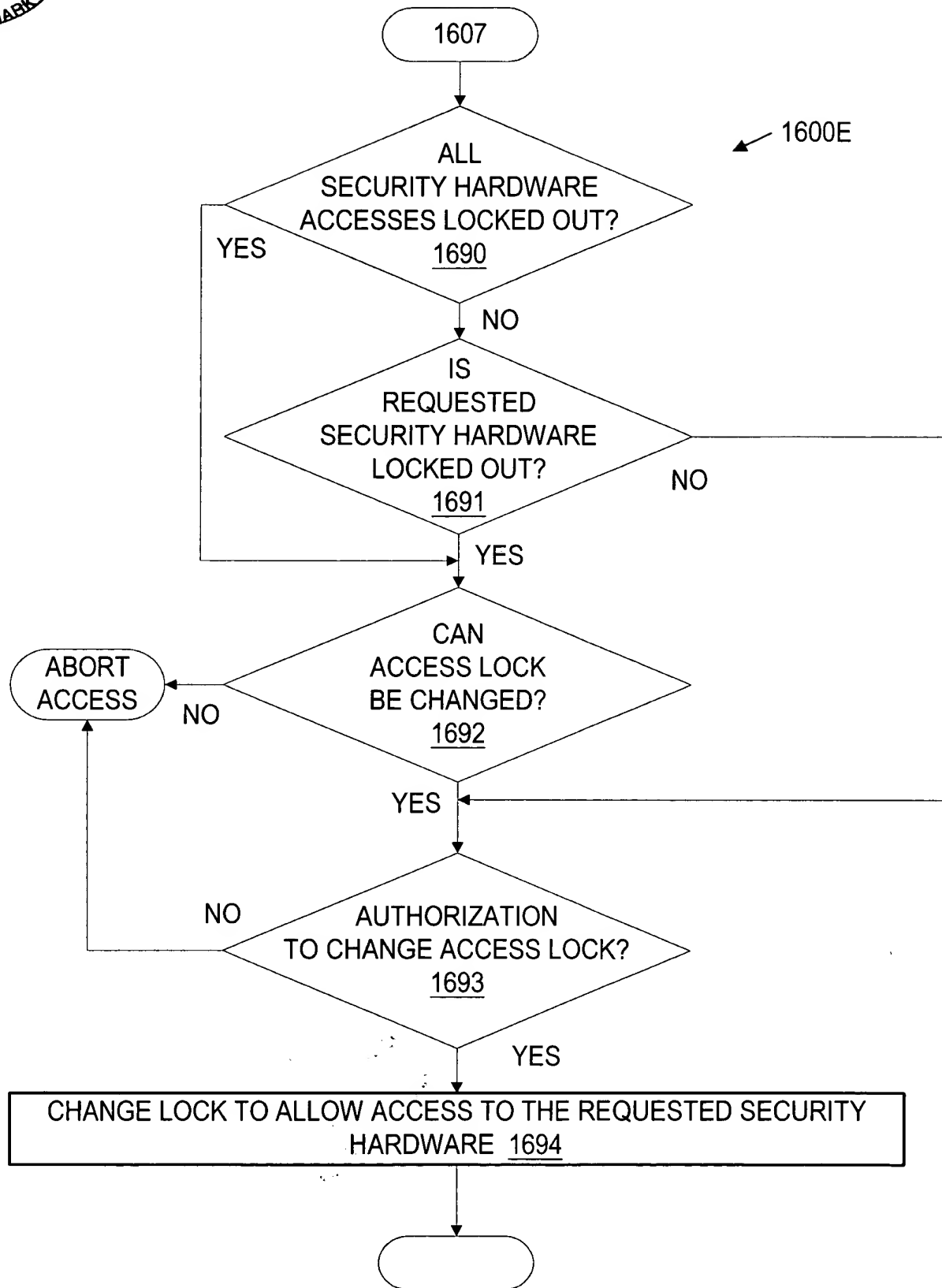


Fig. 16E



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1600F

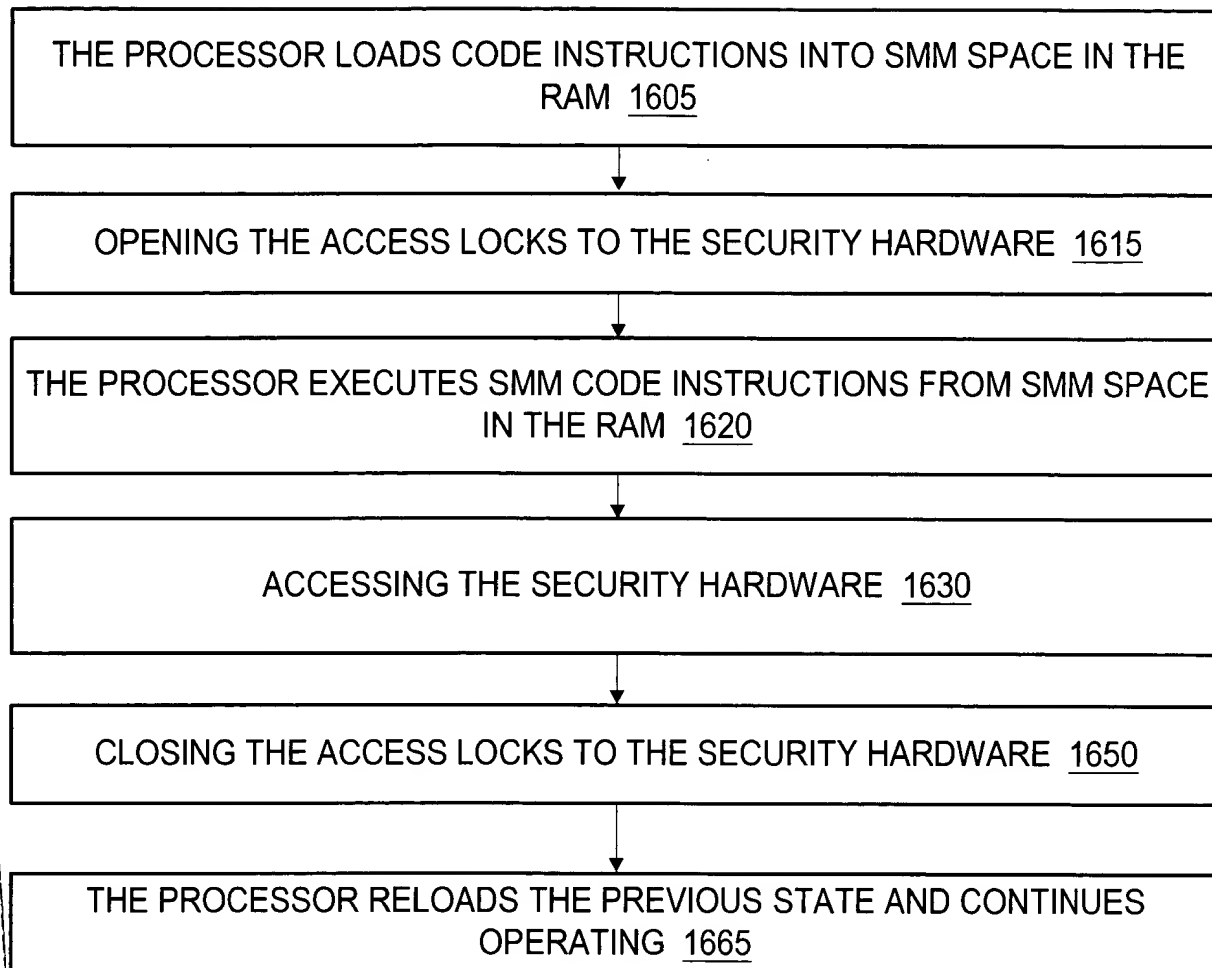


Fig. 16F



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1600G

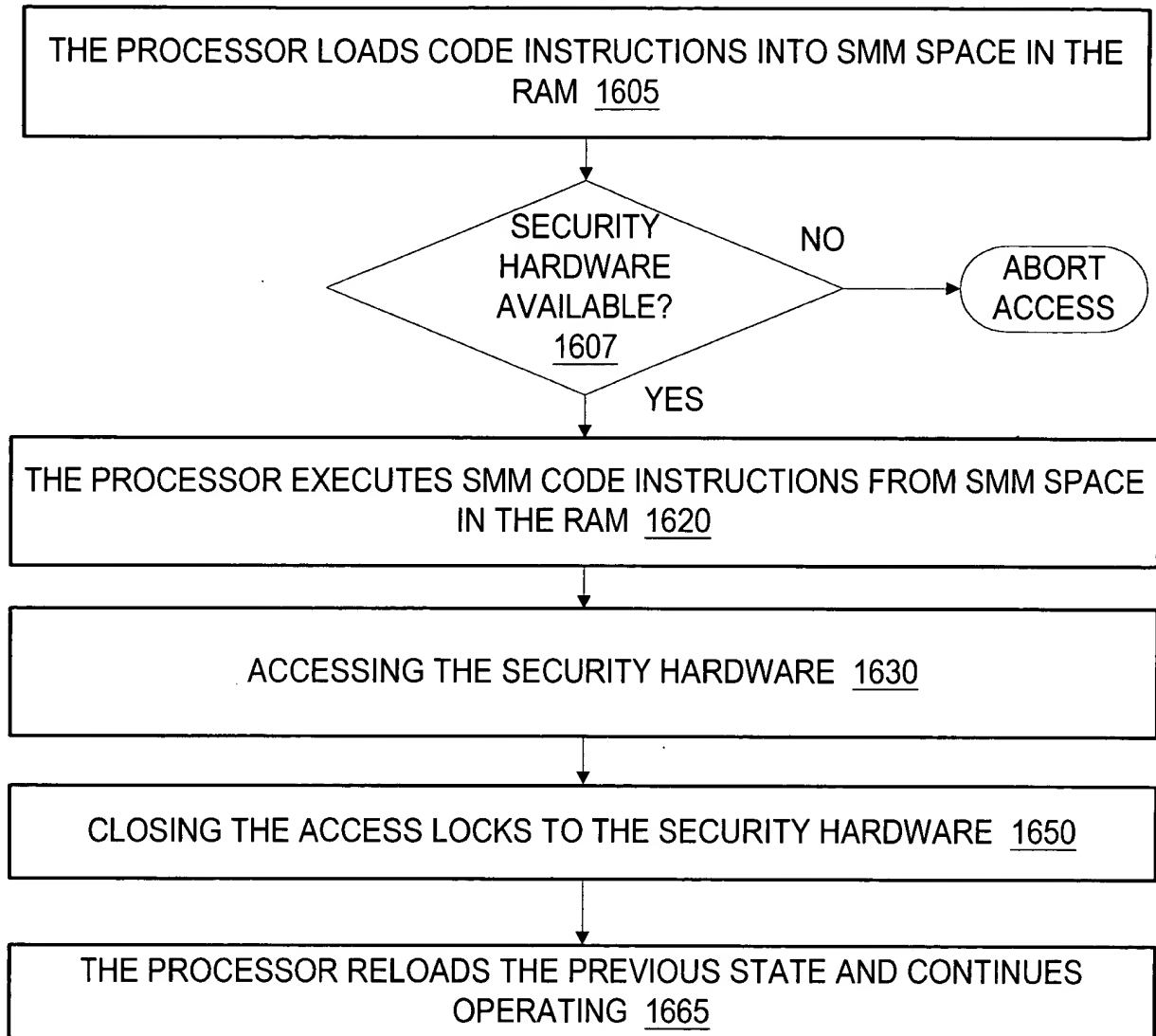


Fig. 16G

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460A

460B

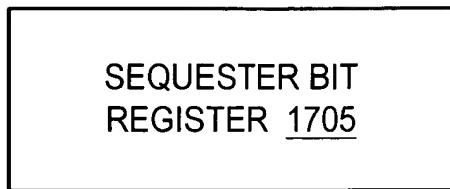


Fig. 17A

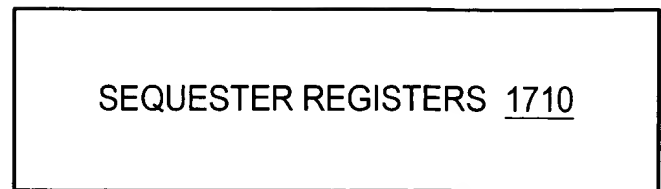


Fig. 17B

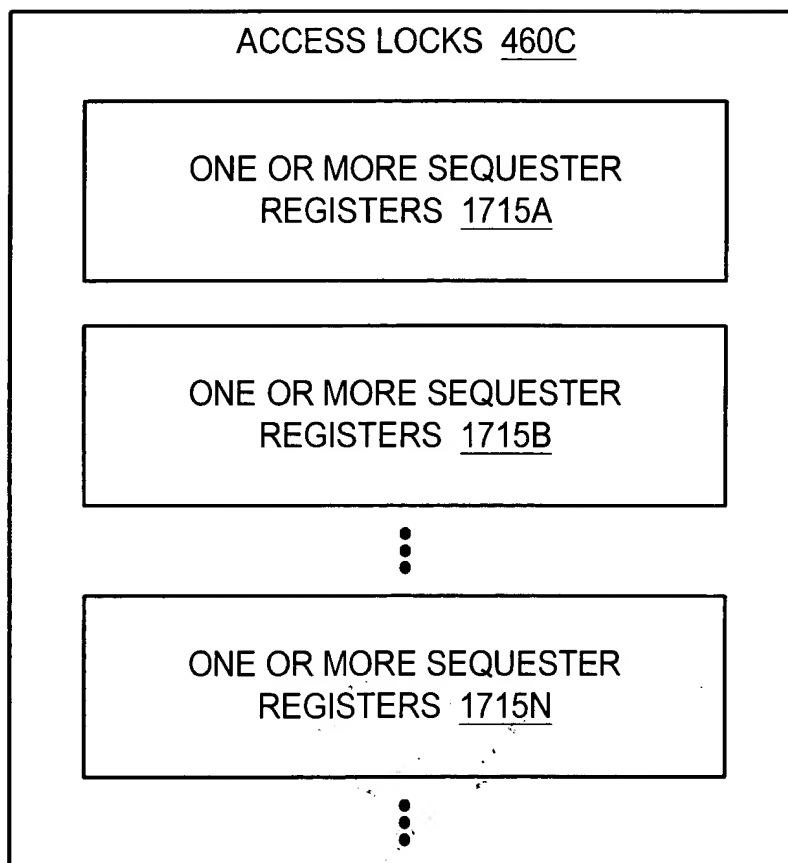


Fig. 17C

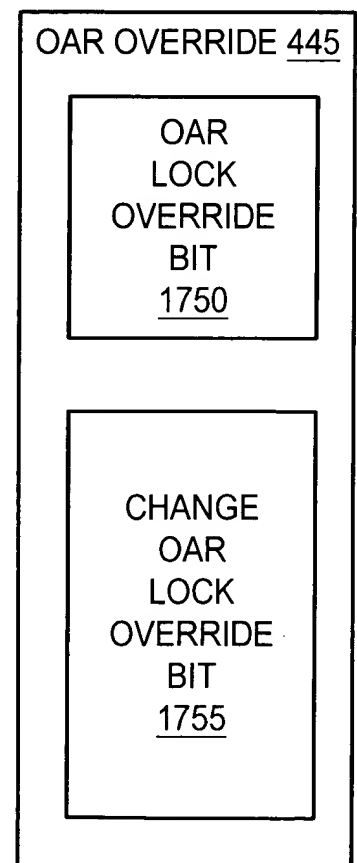


Fig. 17D

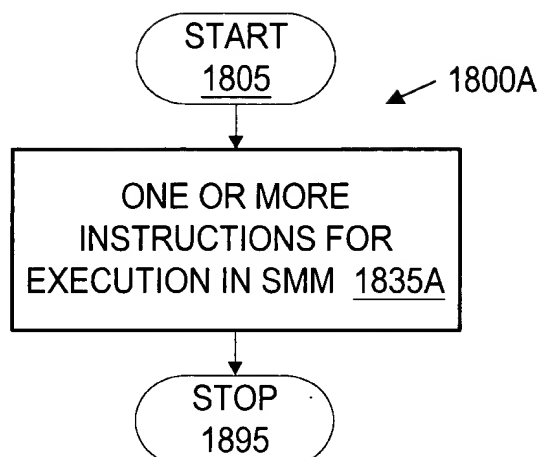


Fig. 18A
PRIOR ART

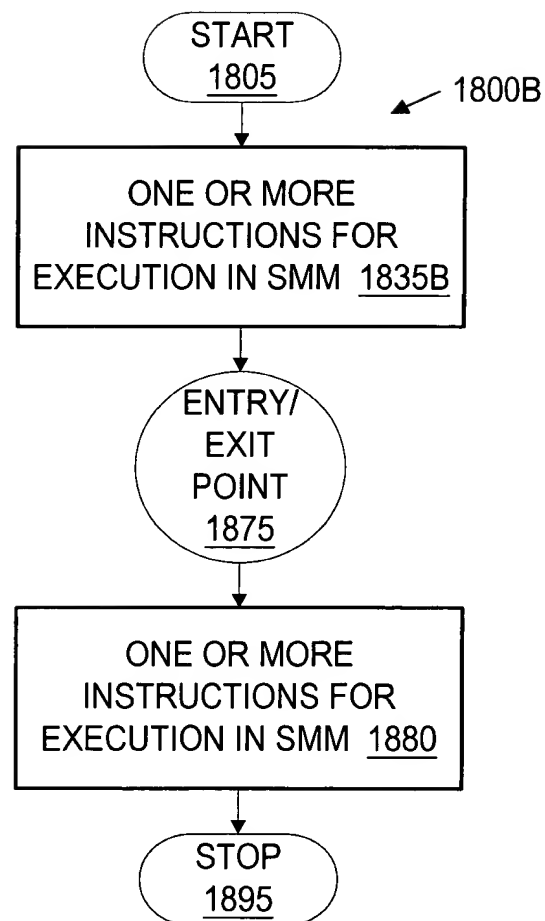


Fig. 18B

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START
1805

1800C

RECEIVE A REQUEST TO ENTER SMM 1810

SAVE SYSTEM STATE 1815

SAVED SMM
STATE? 1820LOAD REQUESTED DEFAULT SMM
STATE 1825

LOAD SAVED SMM STATE 1830

EXECUTE LOADED SMM STATE 1835

FINISHED? 1840

YES

NO

EXIT? 1845

YES

NO

SAVE CURRENT SMM STATE 1850

EXIT SMM 1855

RELOAD SAVED SYSTEM STATE 1860

STOP
1895

Fig. 18C



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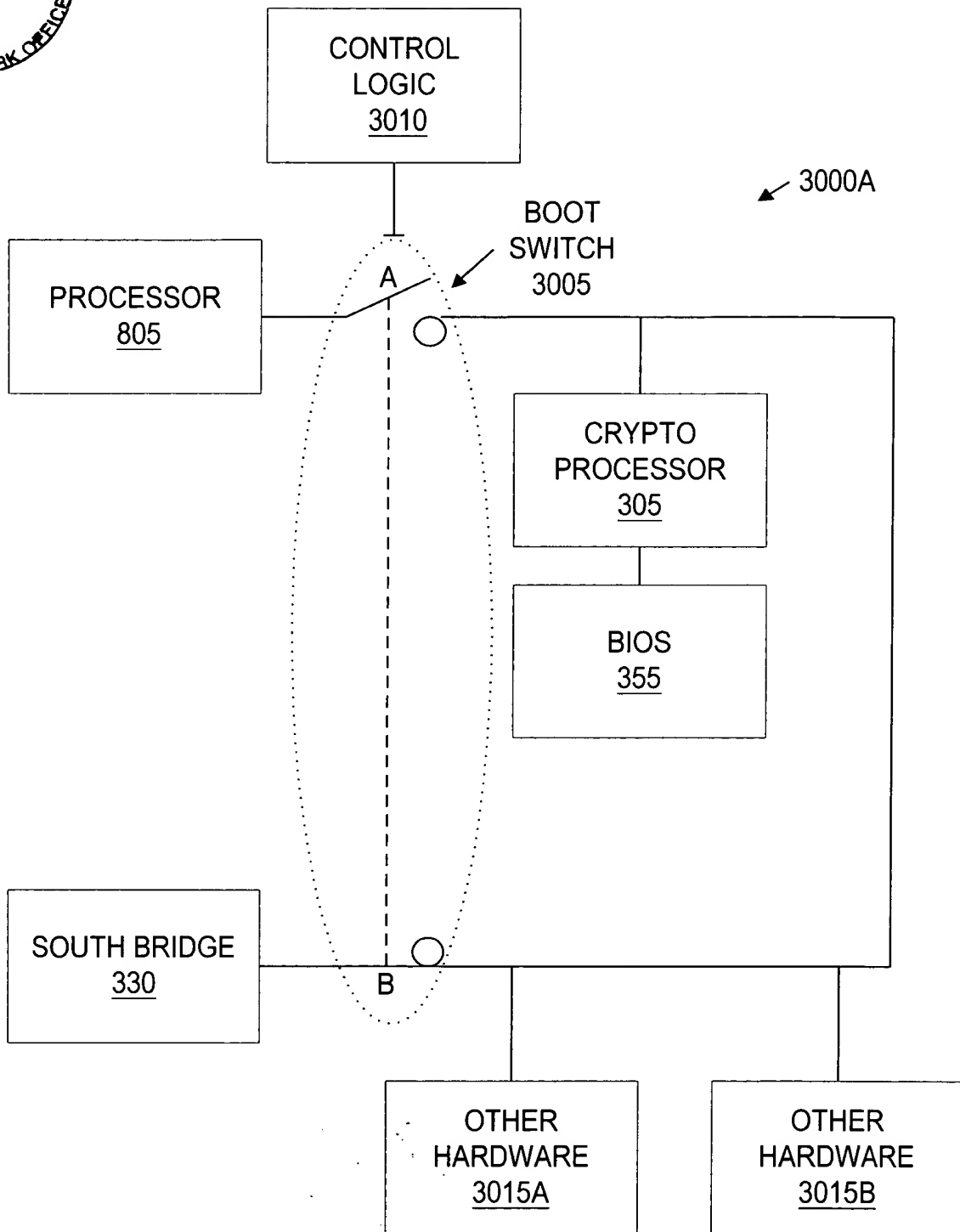


Fig. 19A

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PATENT & TRADEMARK OFFICE

3000B

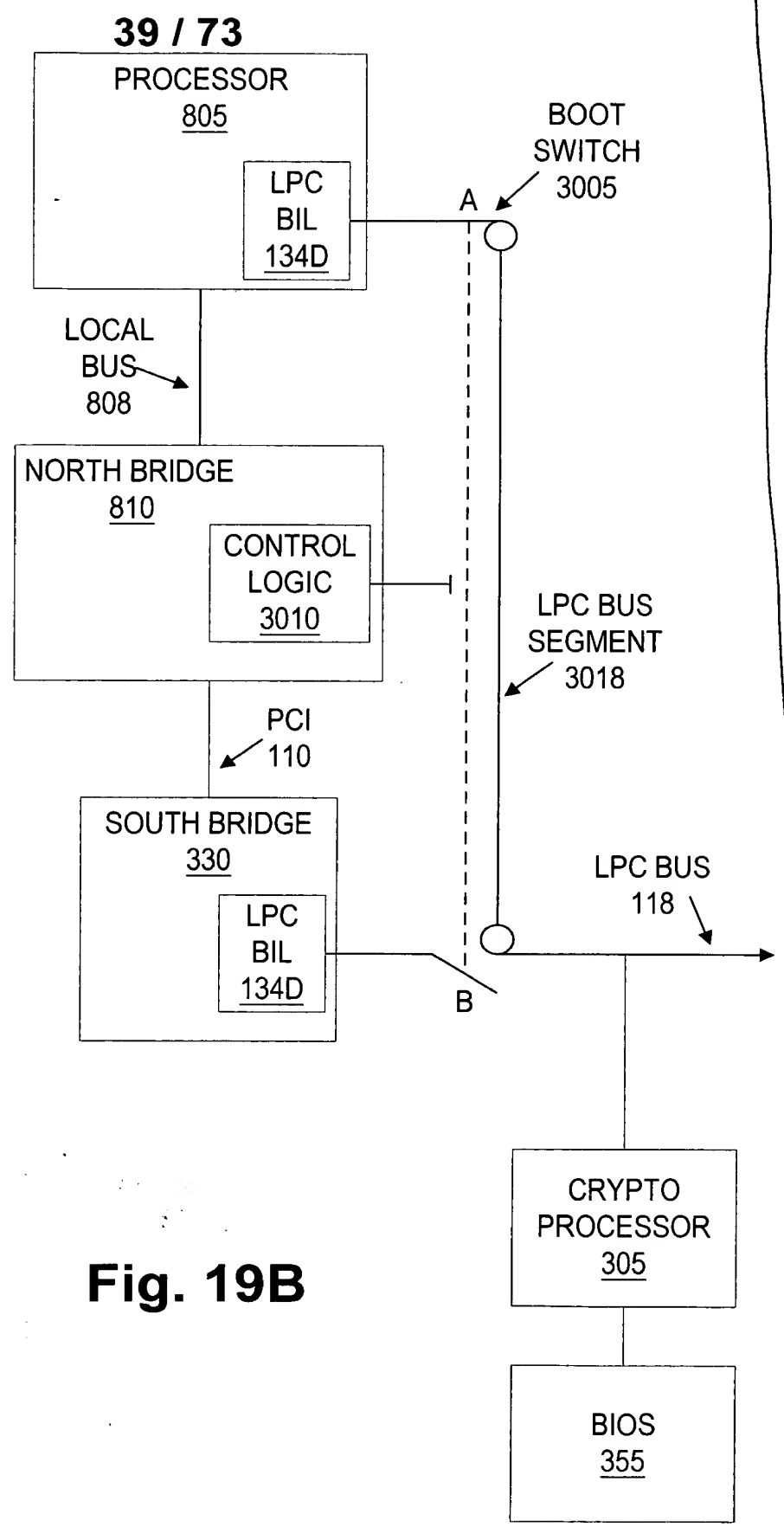
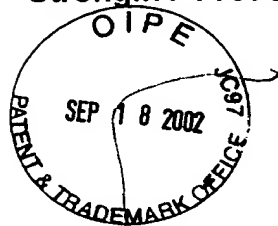


Fig. 19B



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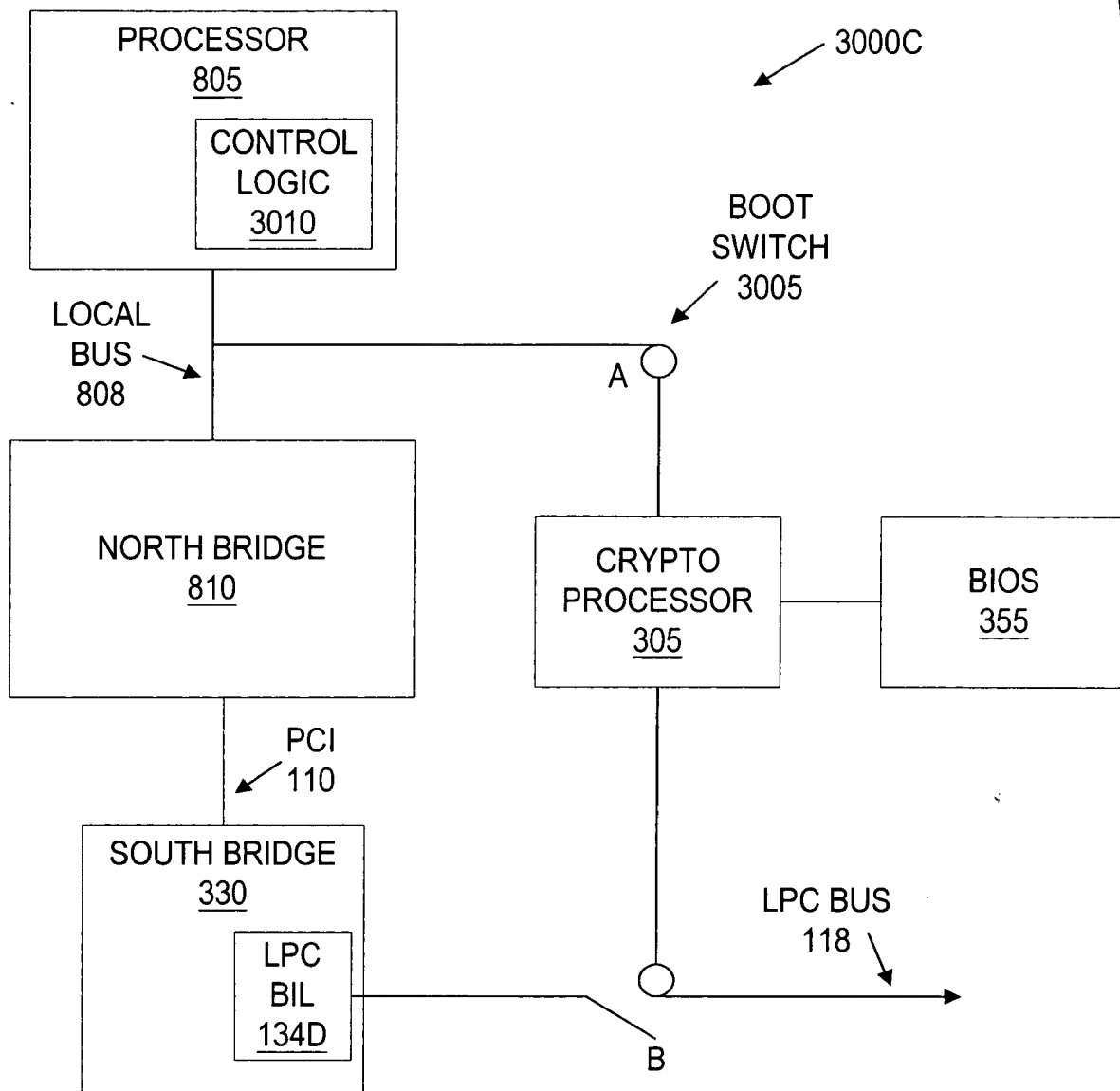


Fig. 19C



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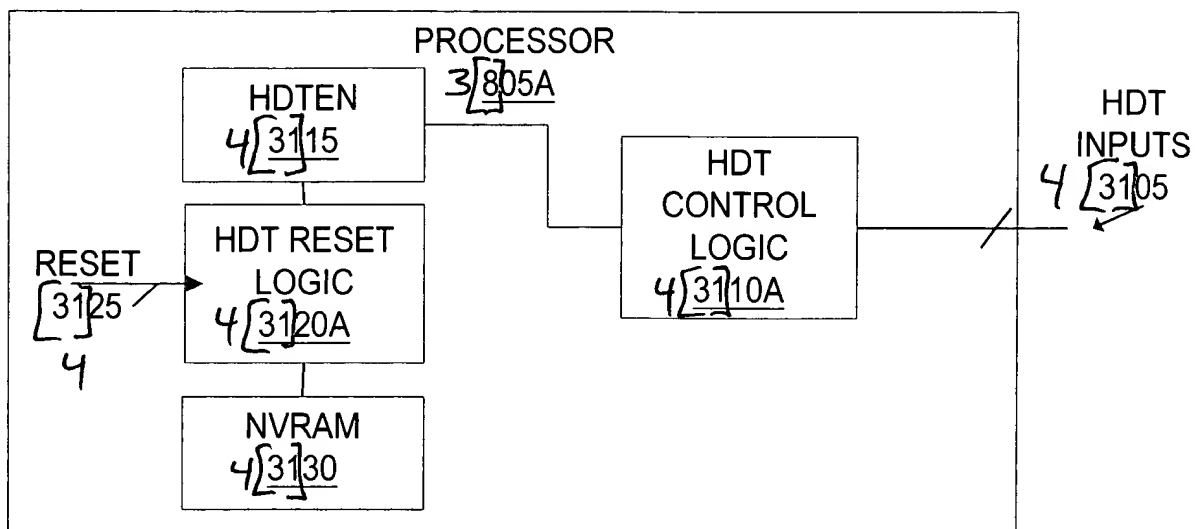


Fig. 20A

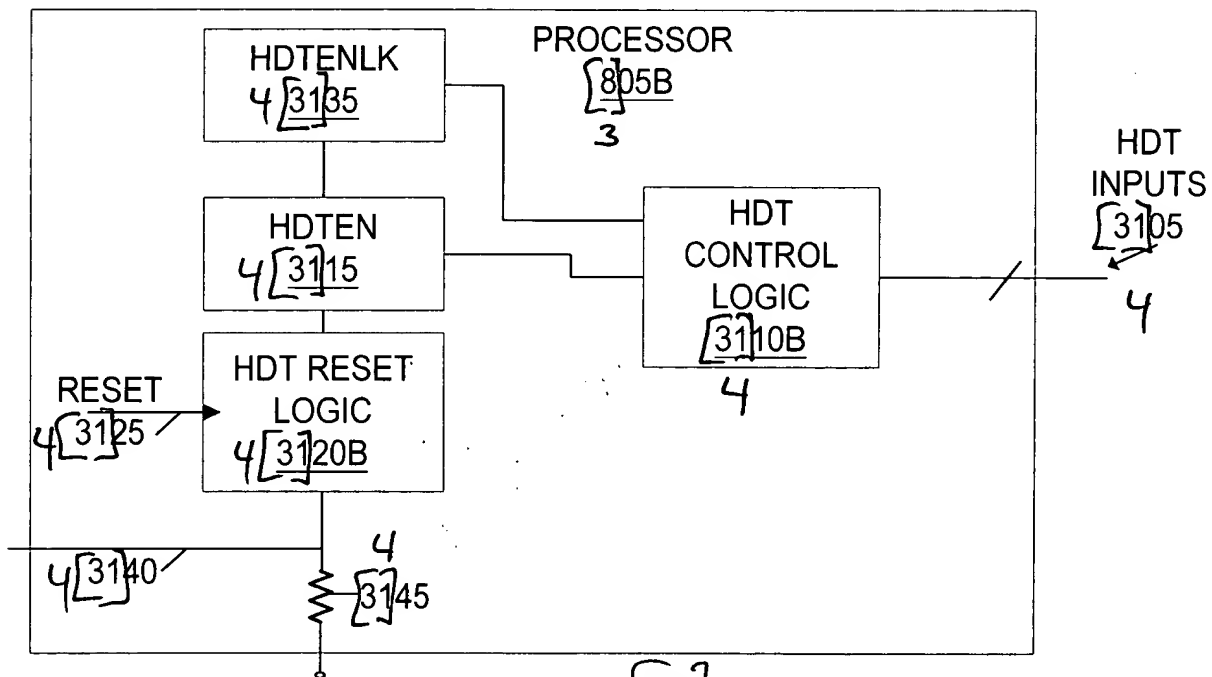
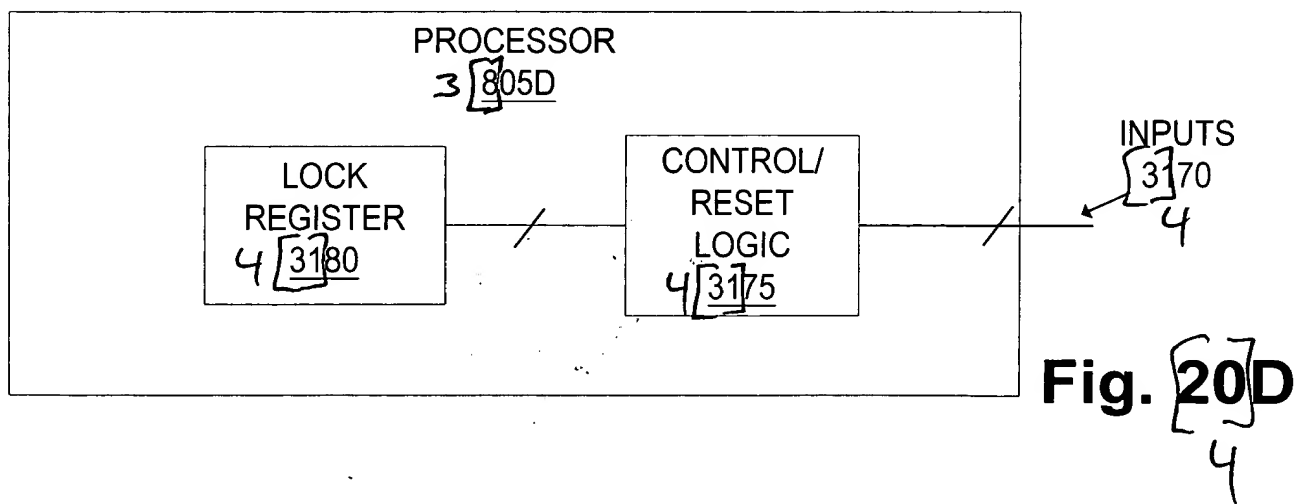
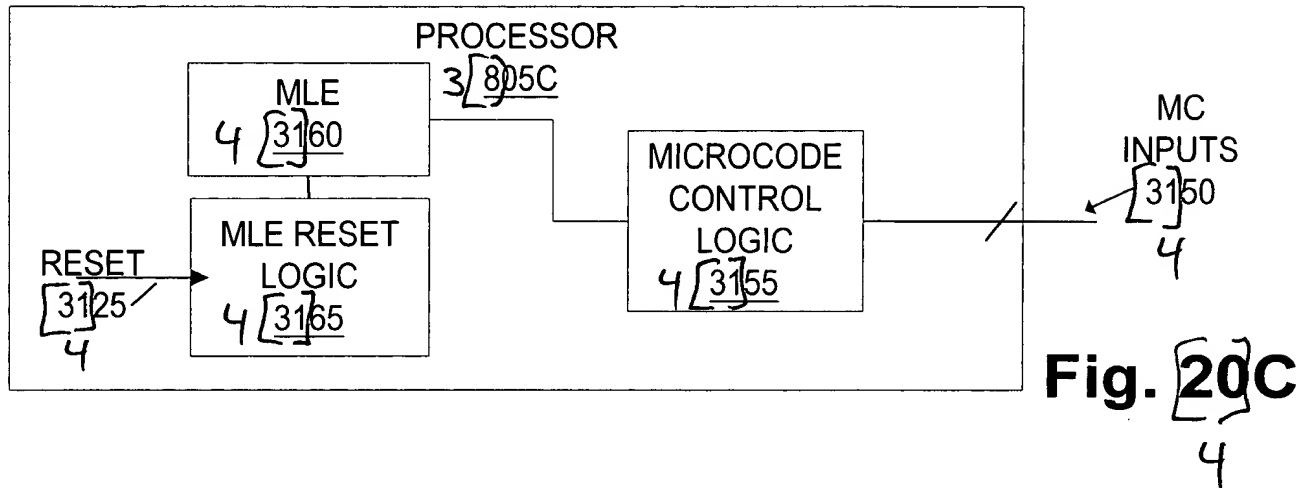


Fig. 20B



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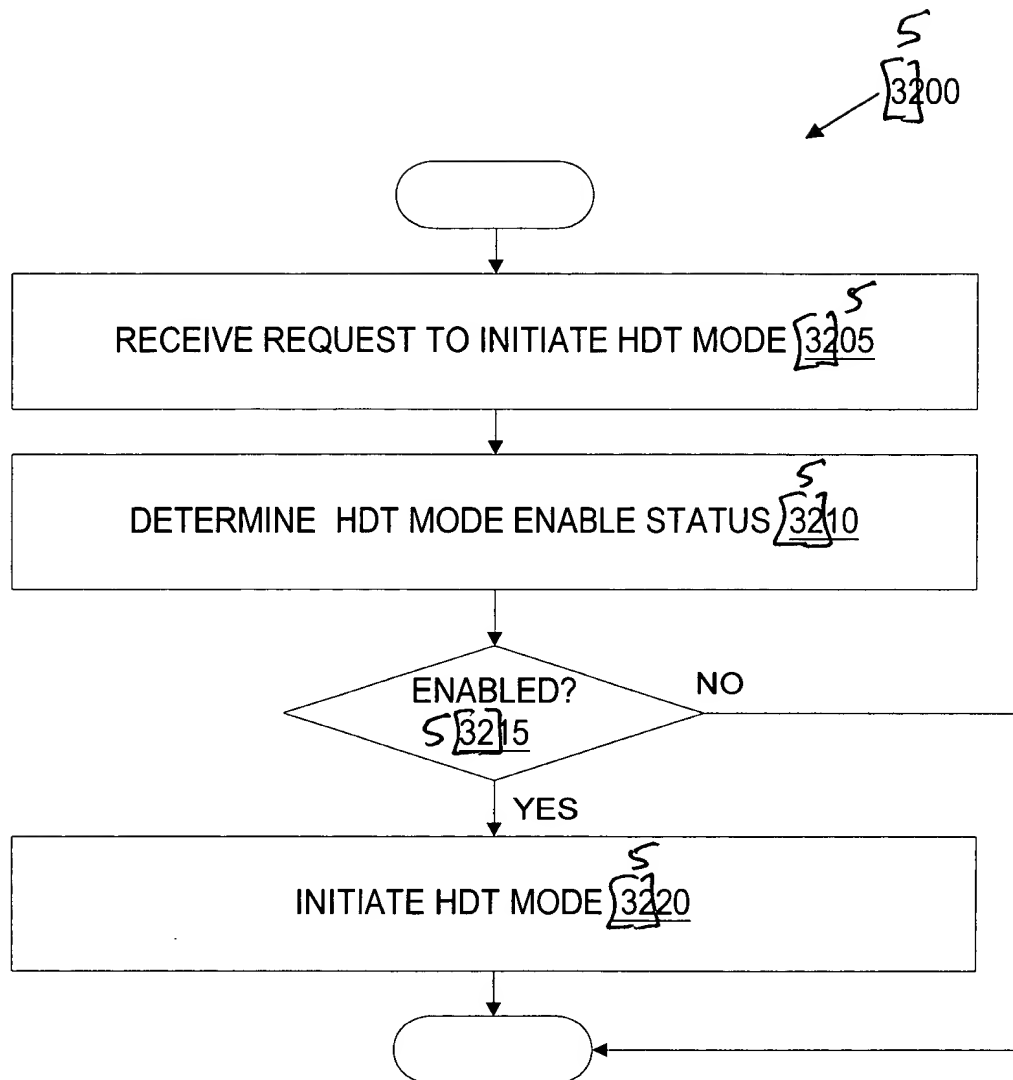


Fig. 21 5



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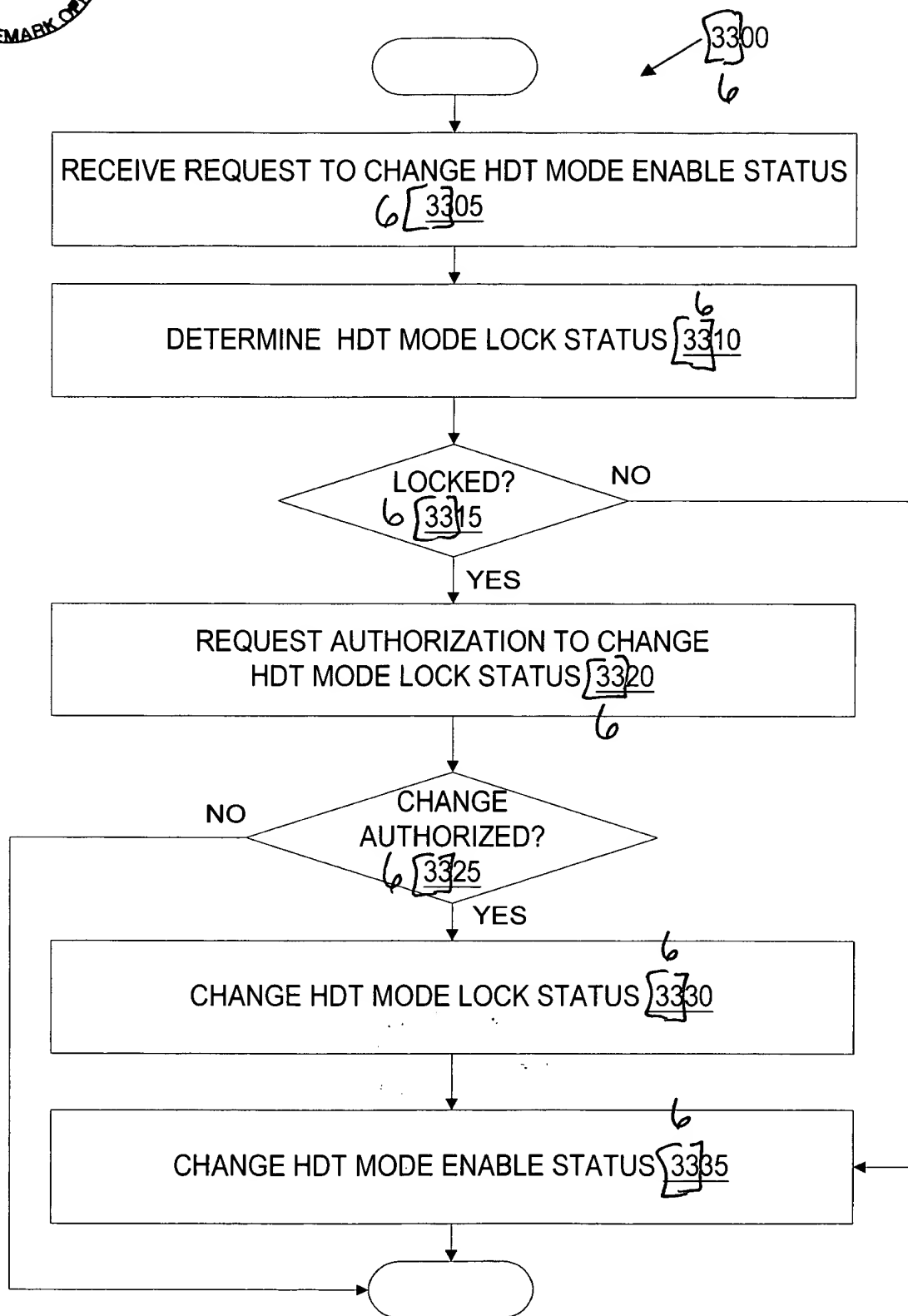


Fig. 22 6



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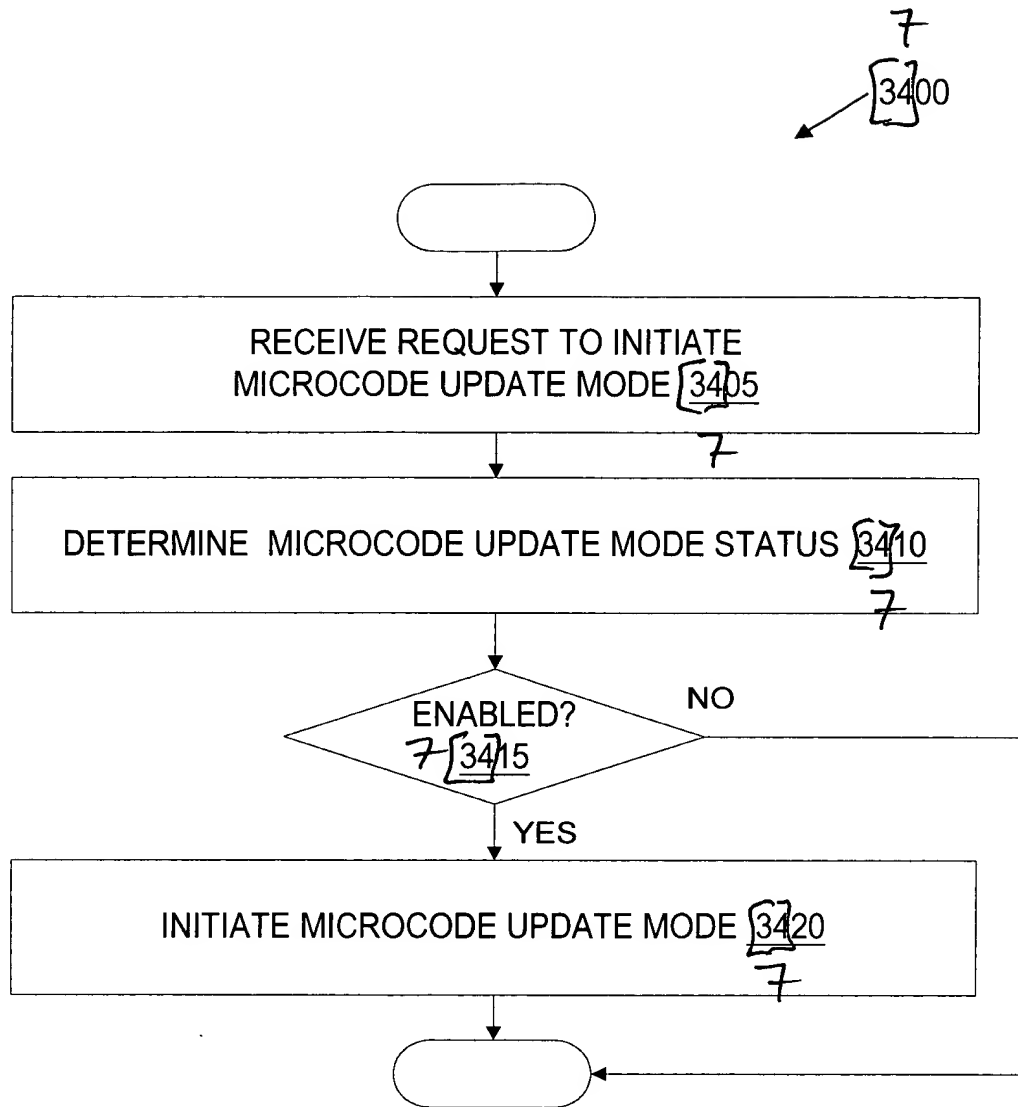


Fig. 23

7



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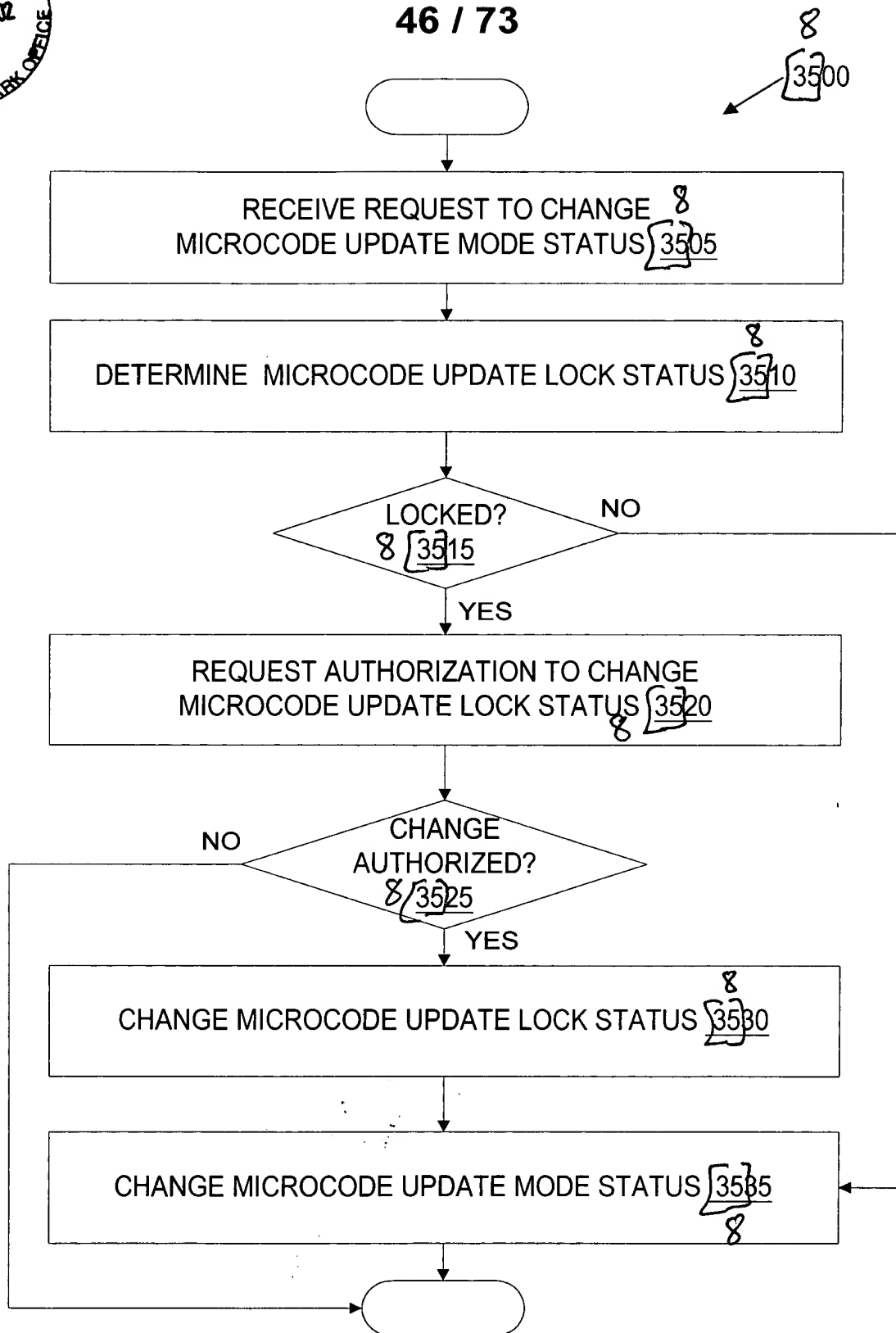
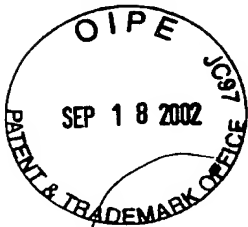


Fig. 24 } 8



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3600A

A SECURITY DEVICE RECEIVES A TRANSACTION REQUEST FOR A STORAGE LOCATION ASSOCIATED WITH A STORAGE DEVICE CONNECTED TO THE SECURITY DEVICE 3605A

THE SECURITY DEVICE PROVIDES ACCESS CONTROL FOR THE STORAGE DEVICE 3610A

THE SECURITY DEVICE MAPS THE STORAGE LOCATION IN THE TRANSACTION REQUEST ACCORDING TO THE ADDRESS MAPPING OF THE STORAGE DEVICE 3615A

THE SECURITY DEVICE PROVIDES THE TRANSACTION REQUEST TO THE STORAGE DEVICE 3620A

THE STORAGE DEVICE PERFORMS THE REQUESTED TRANSACTION 3625A

Fig. 25A



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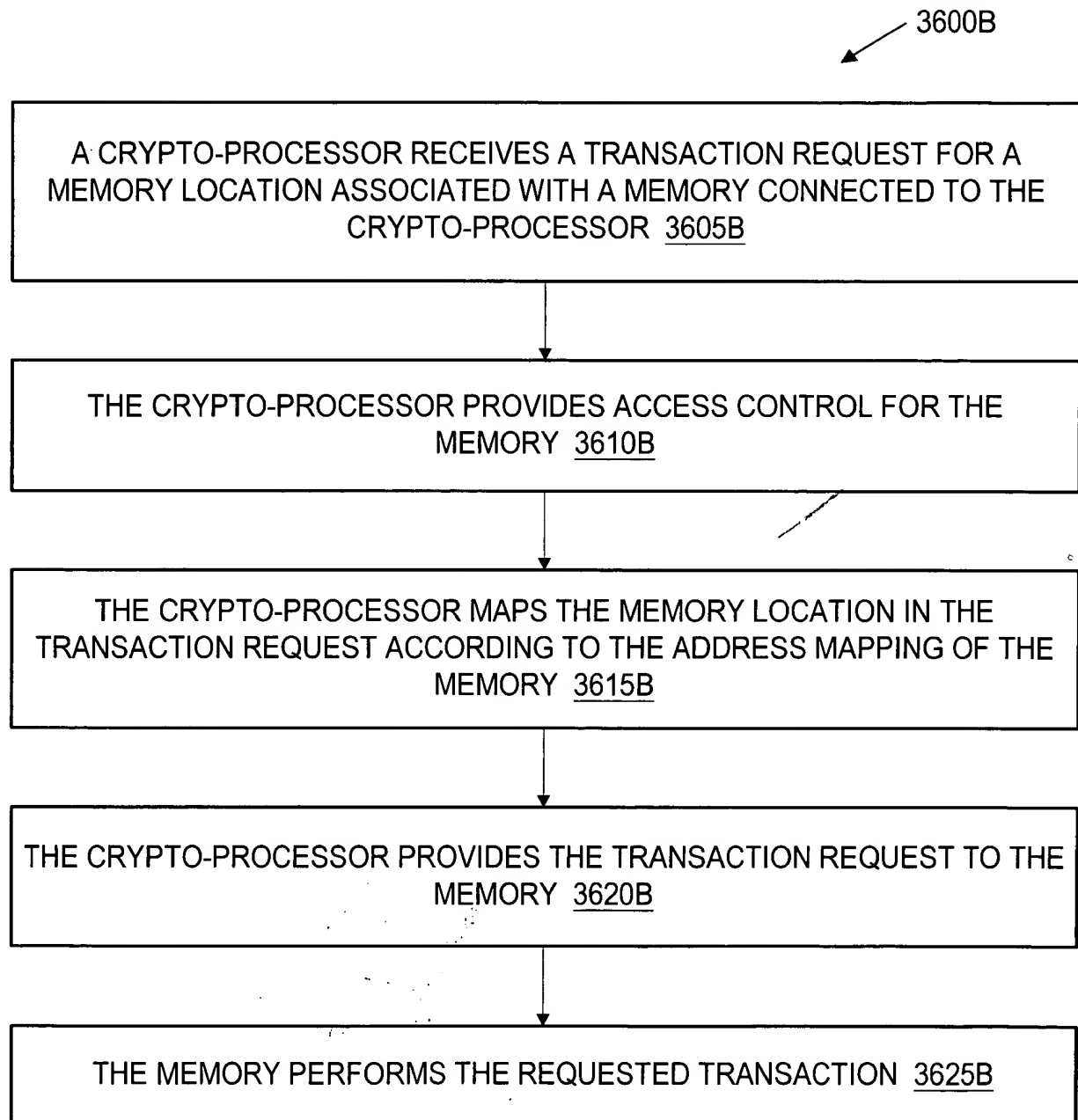


Fig. 25B

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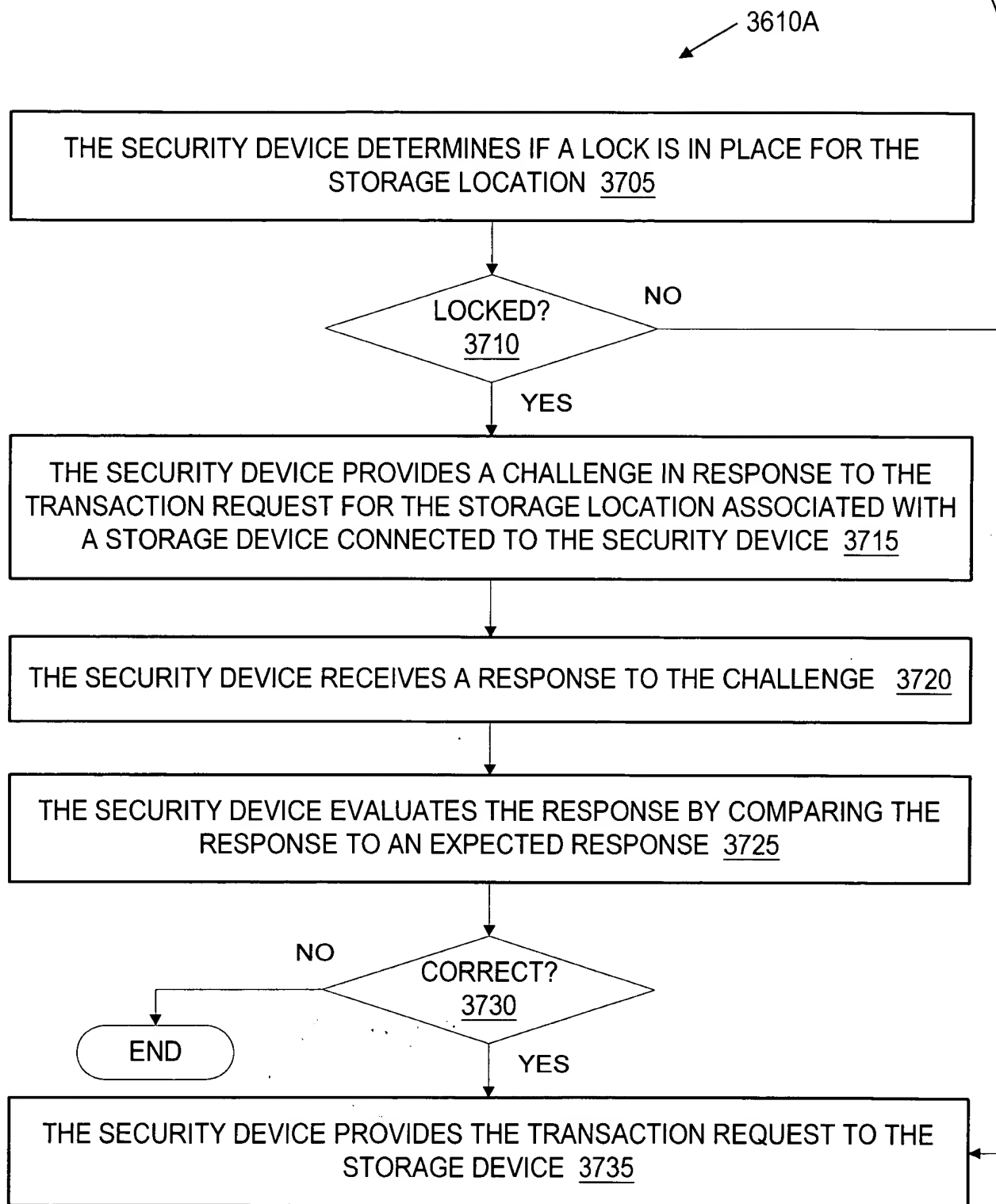


Fig. 26

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3620

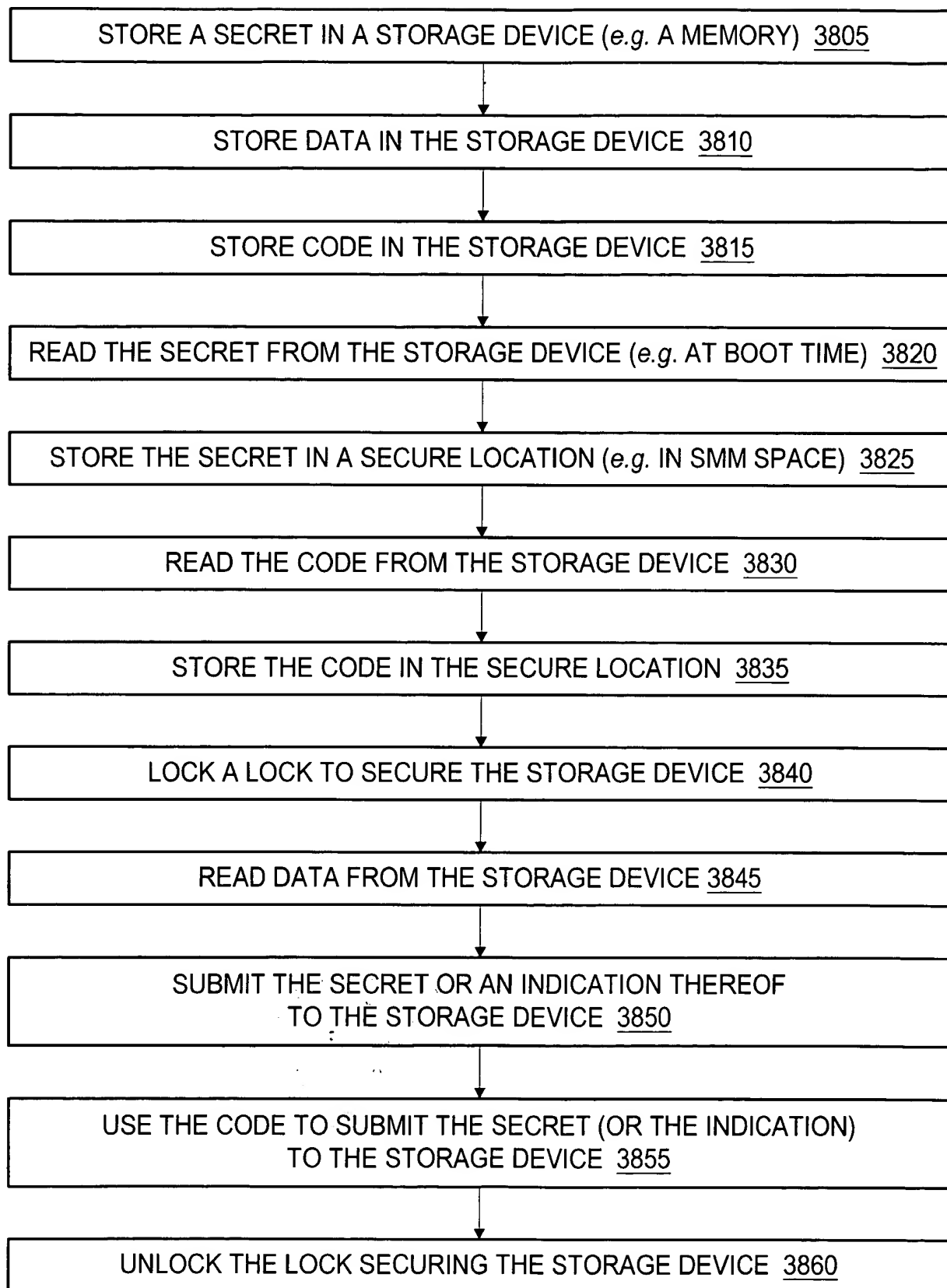
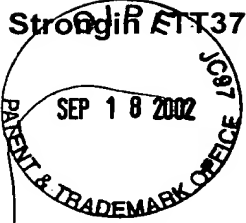


Fig. 27



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3900

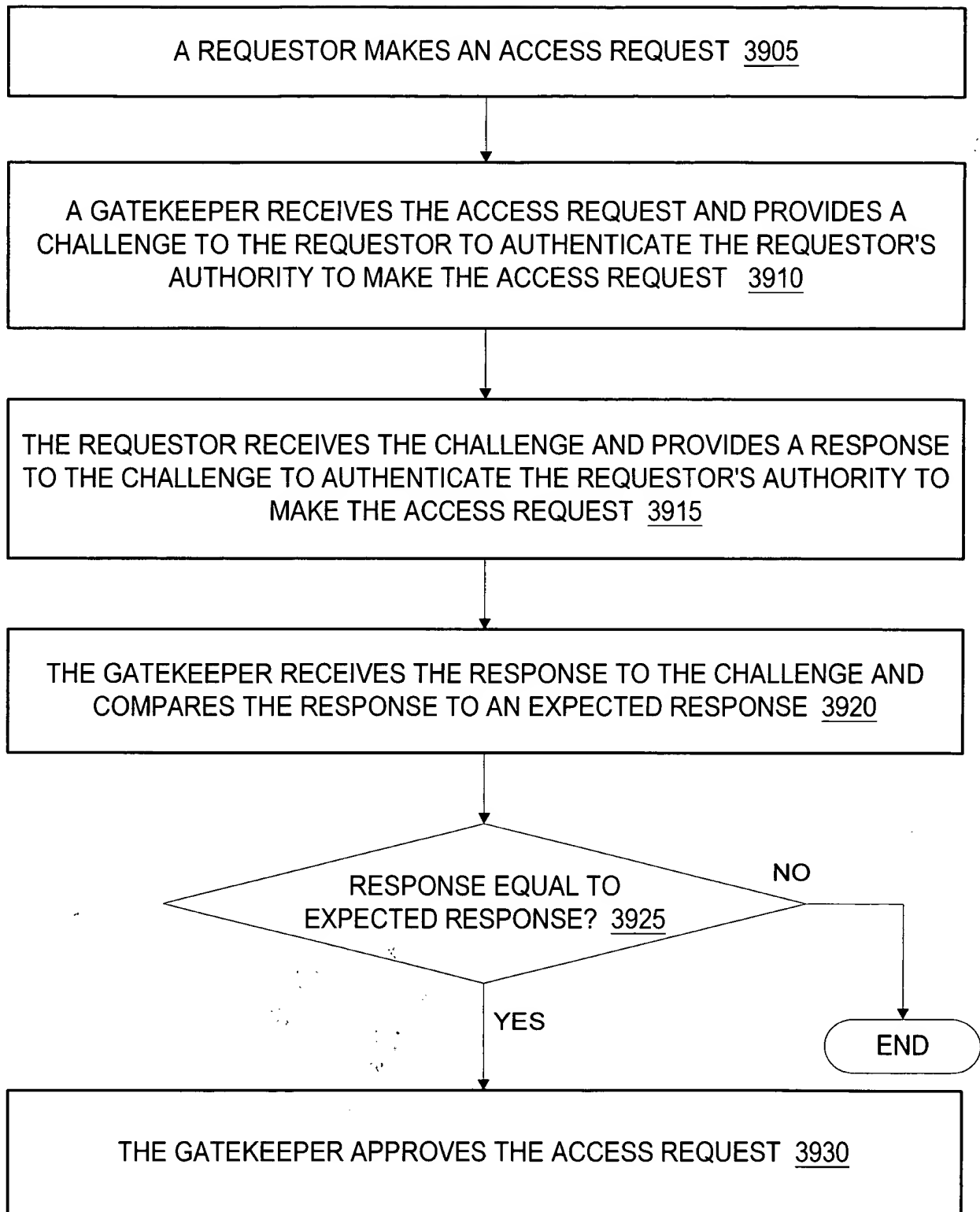
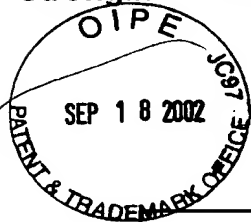


Fig. 28
(Prior Art)



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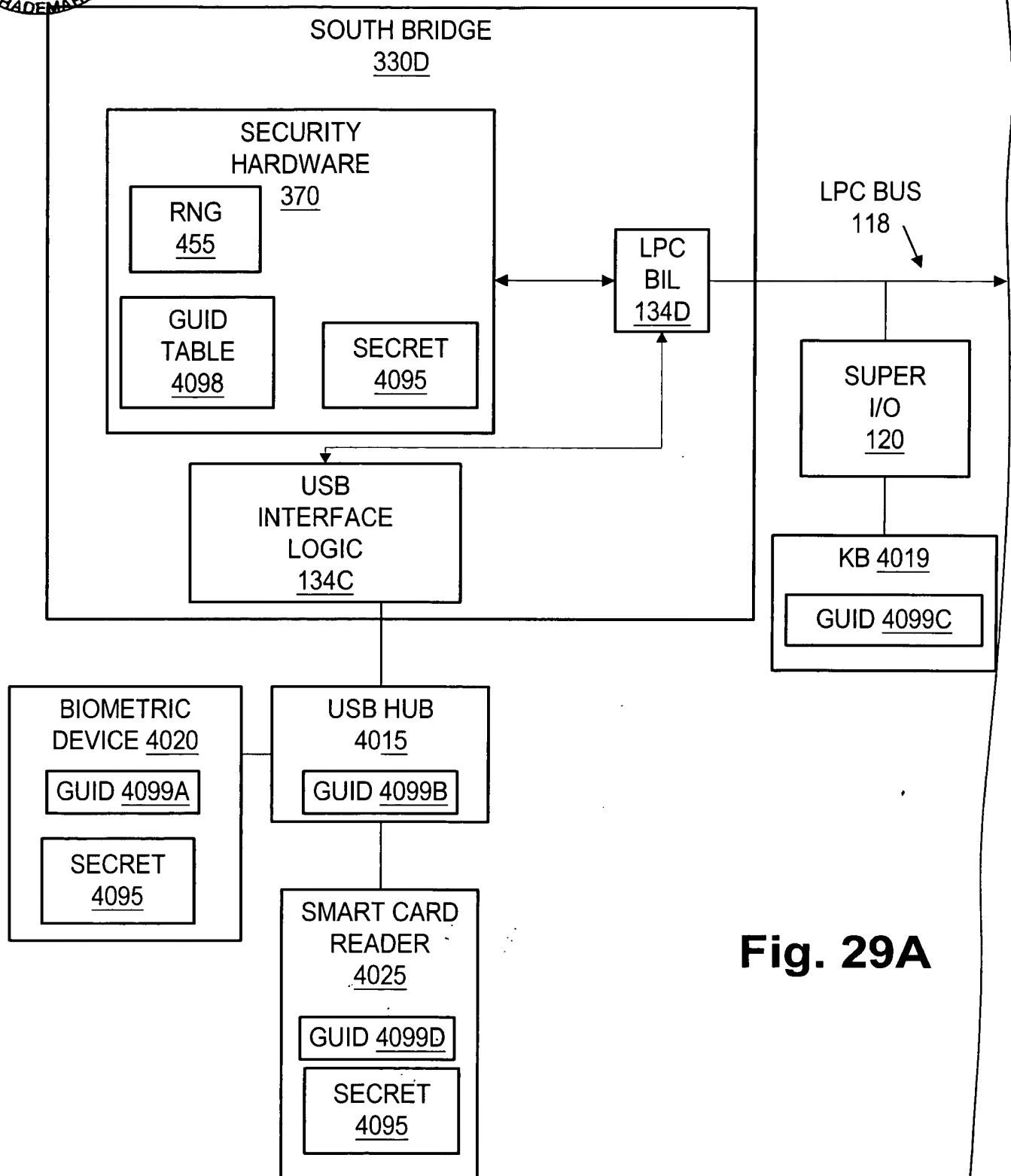


Fig. 29A

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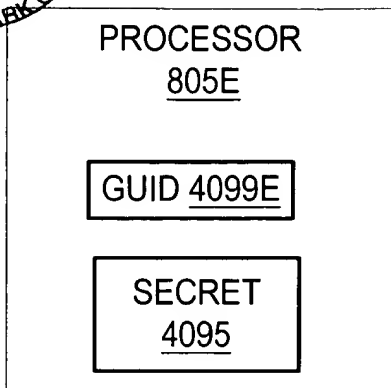


Fig. 29B

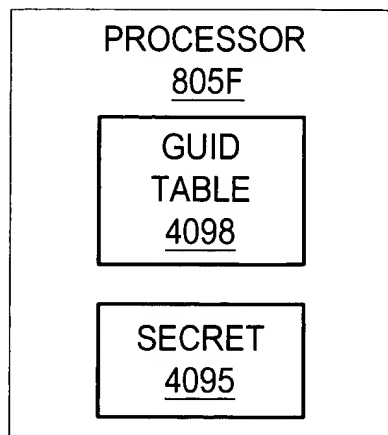


Fig. 29C

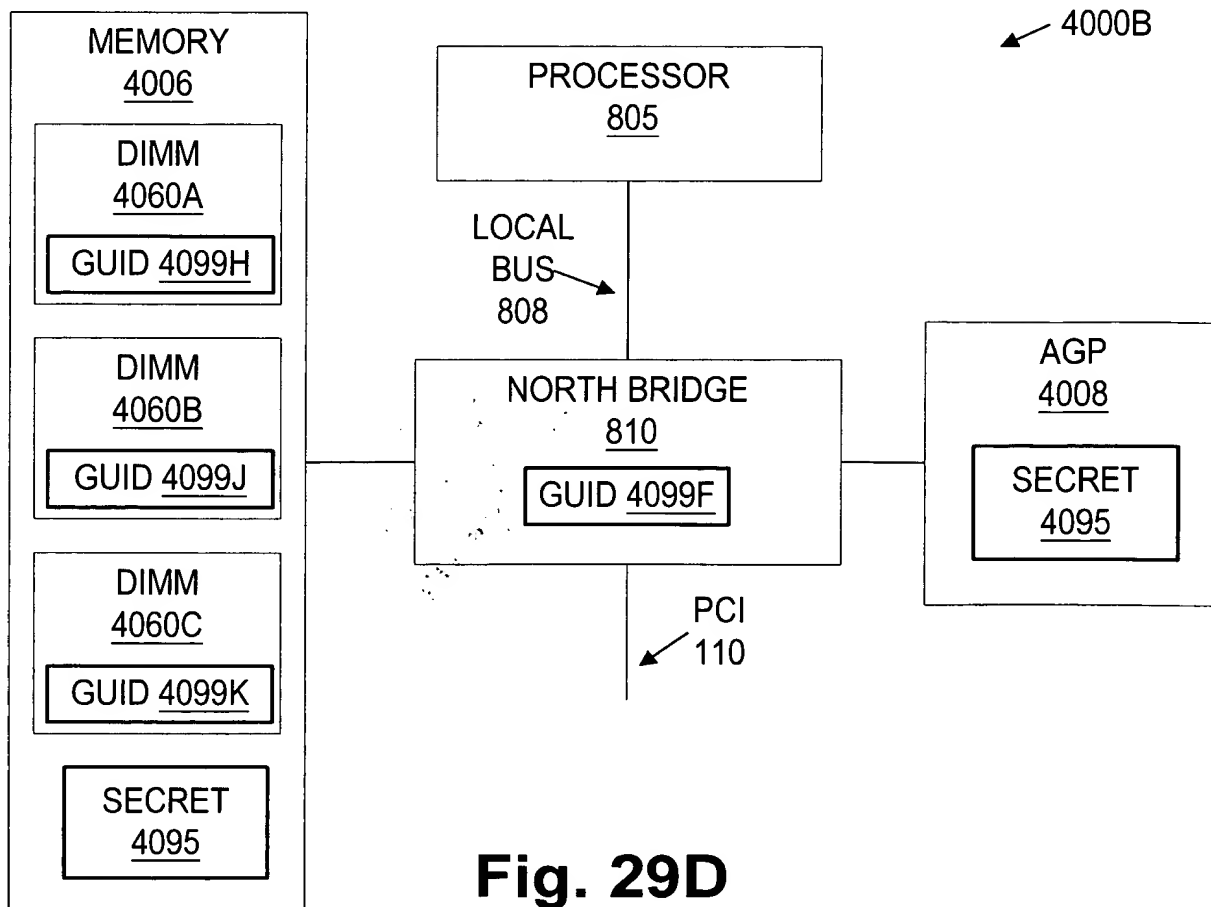


Fig. 29D



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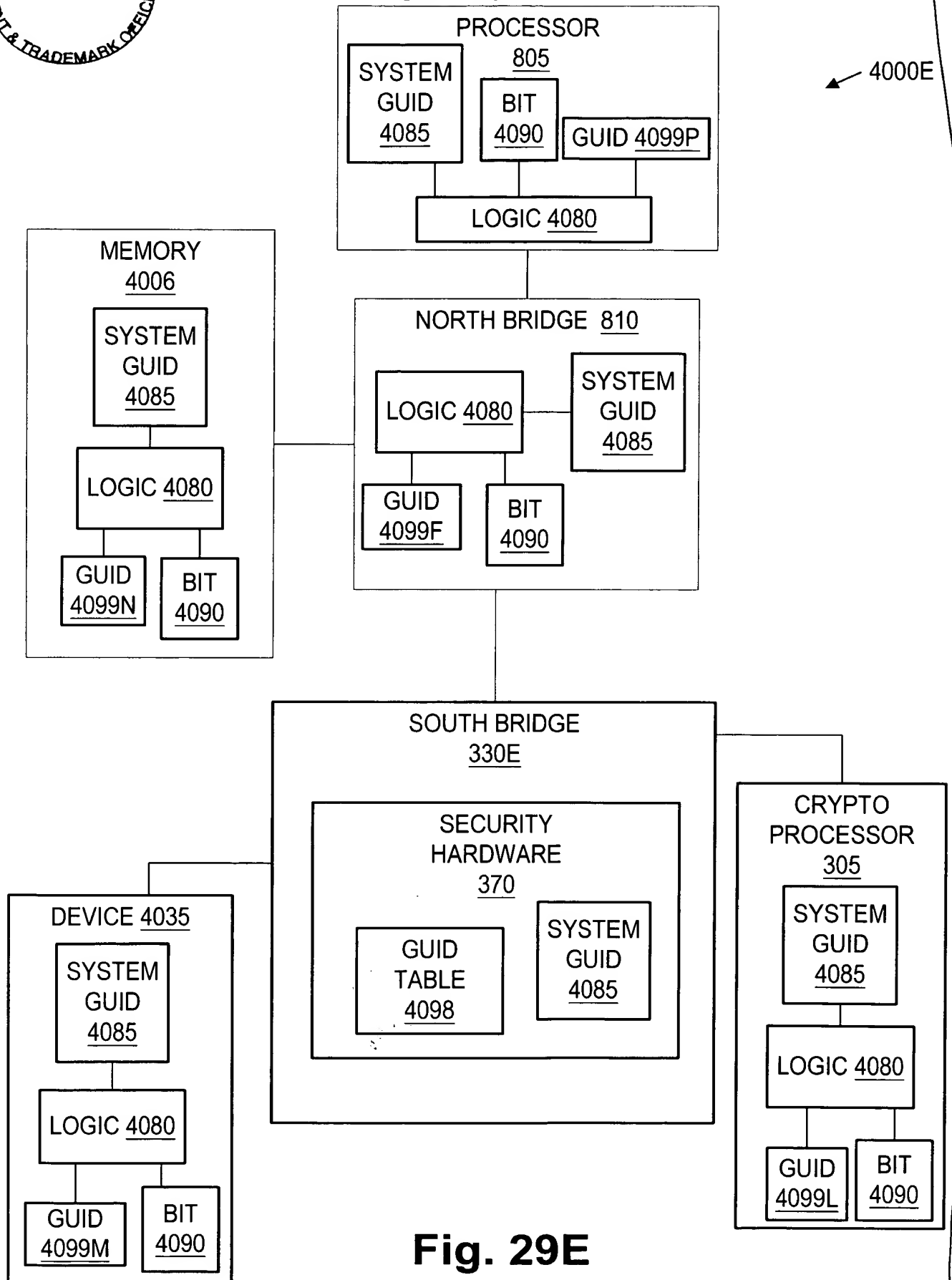


Fig. 29E



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4100A

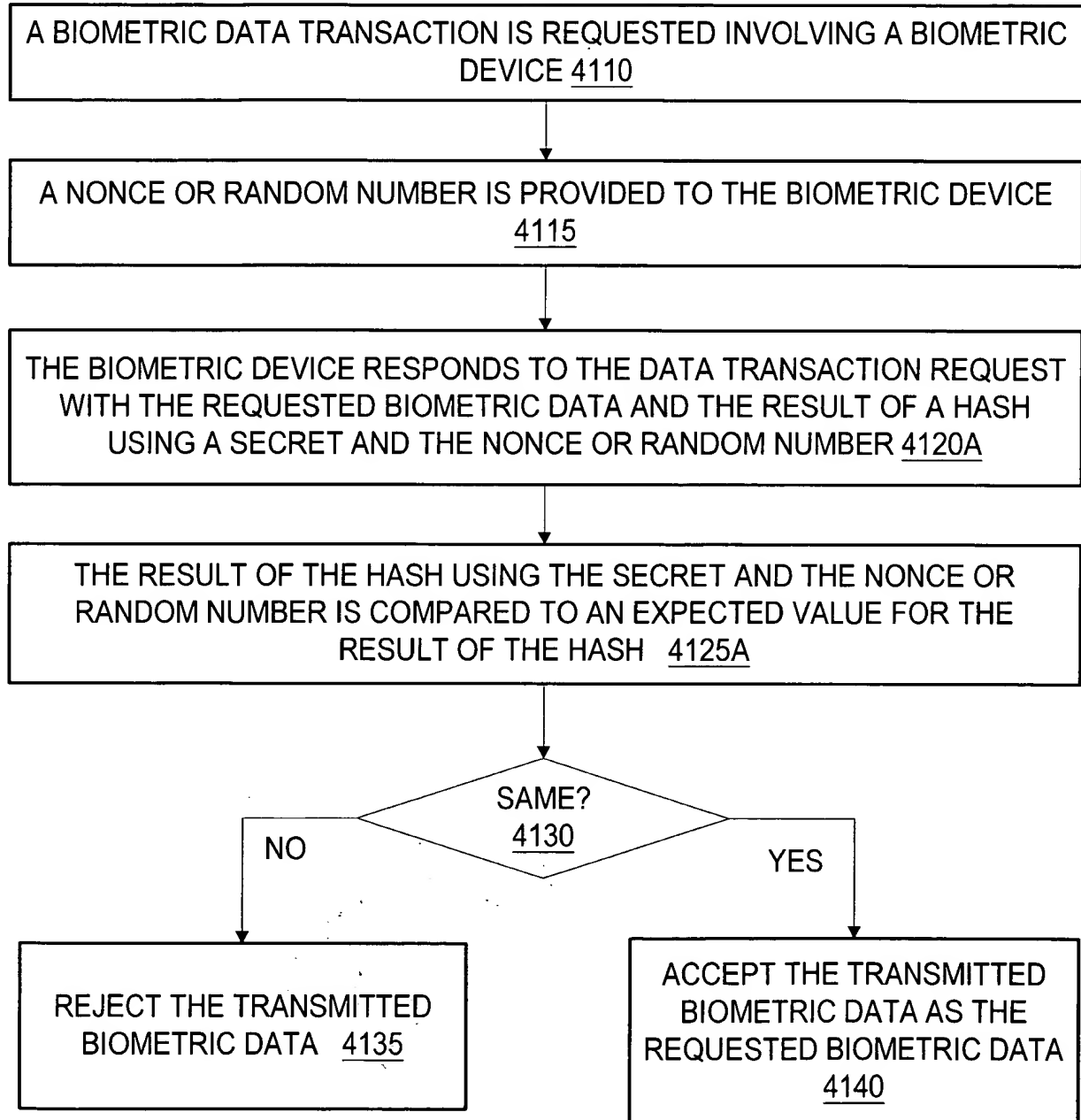


Fig. 30A

4100B

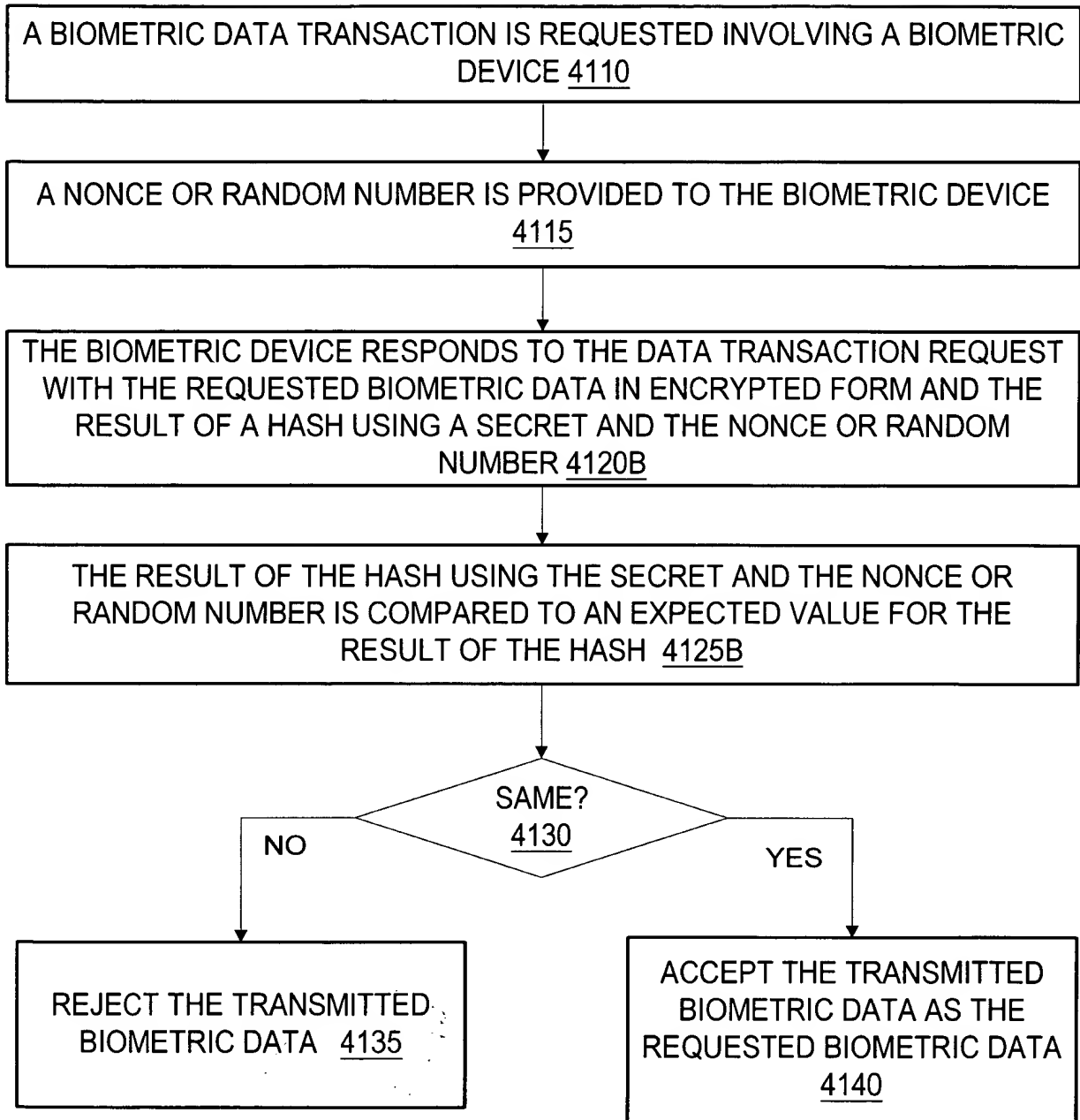


Fig. 30B

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4200A

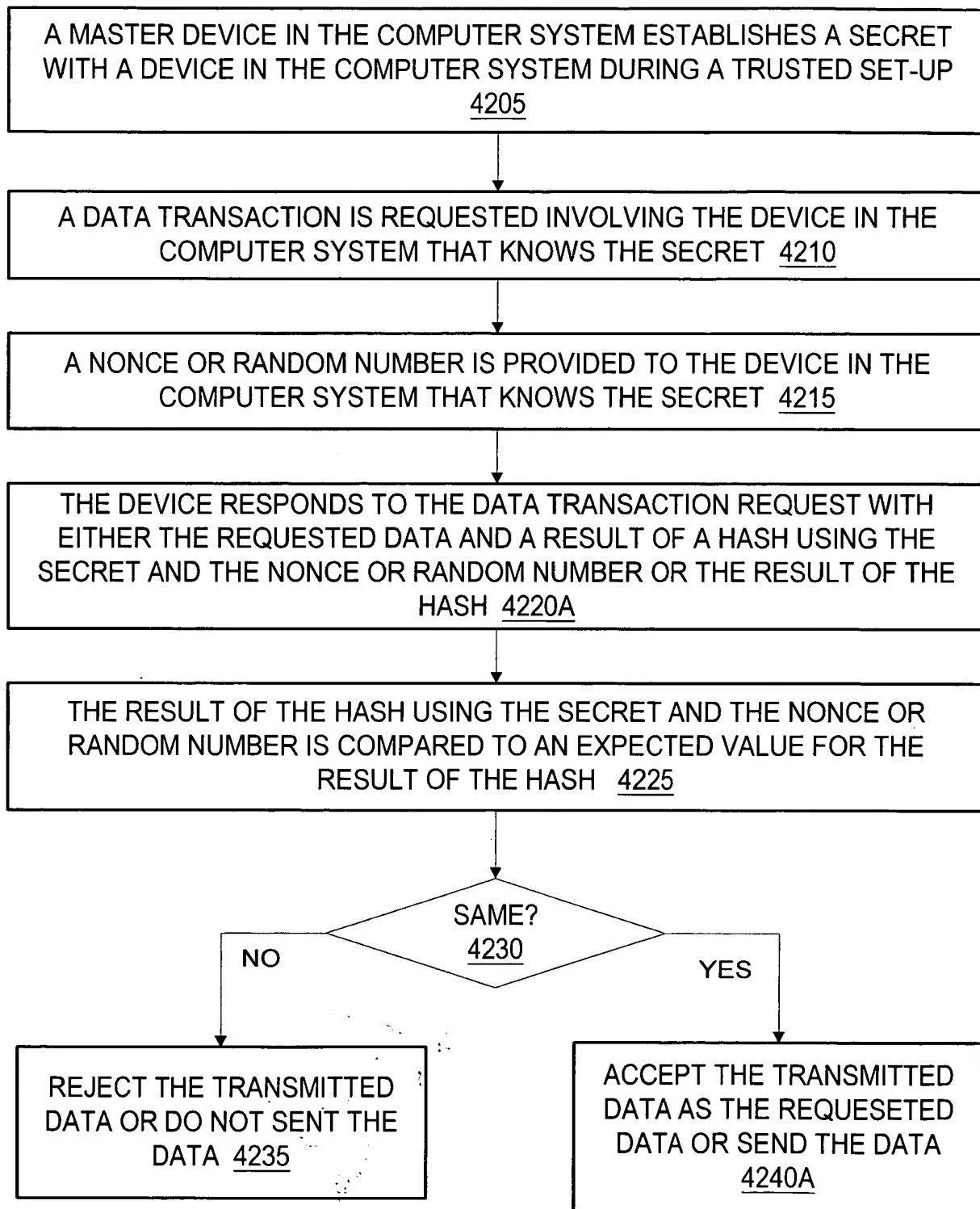


Fig. 31A

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4200B

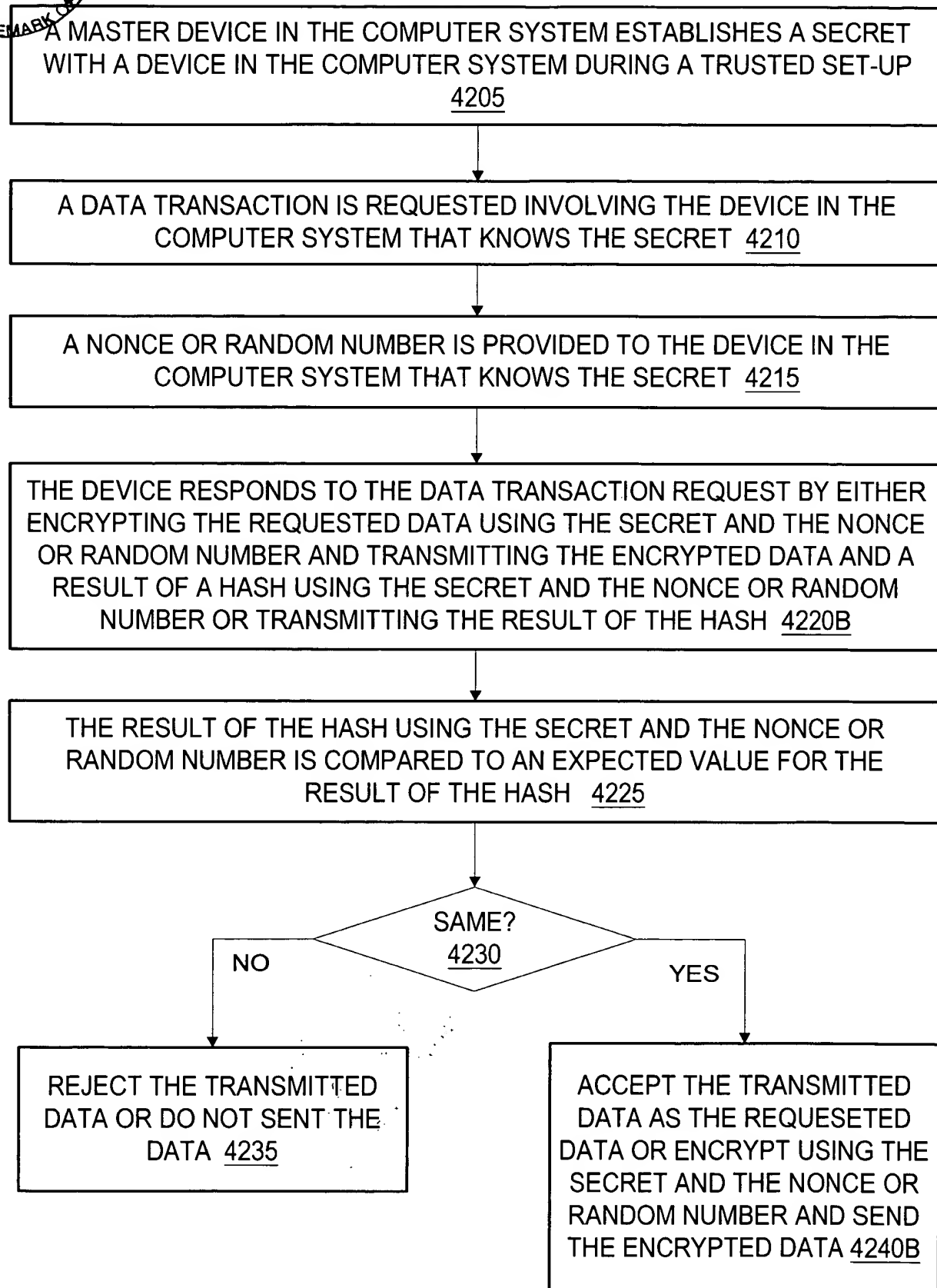


Fig. 31B

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4300A

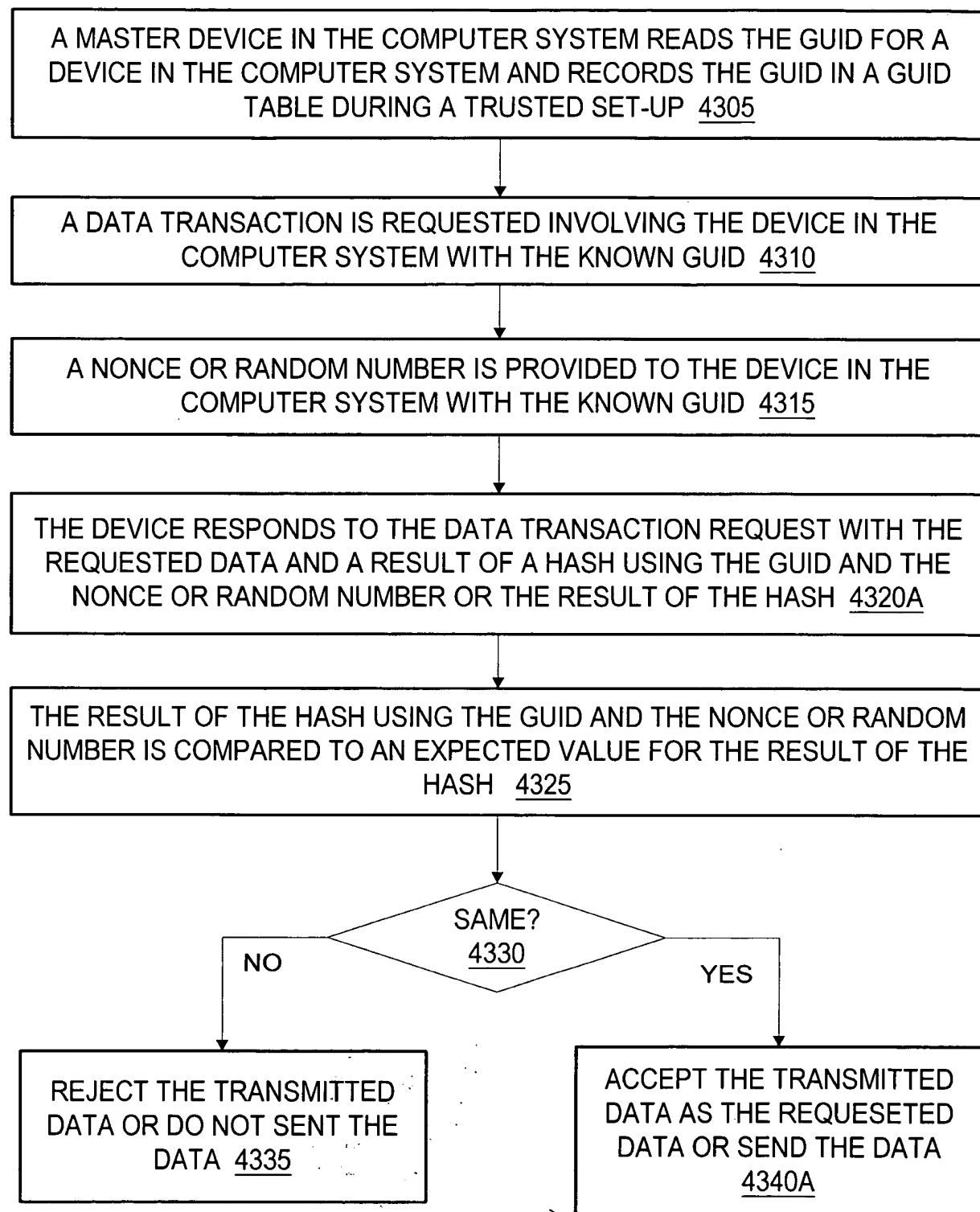
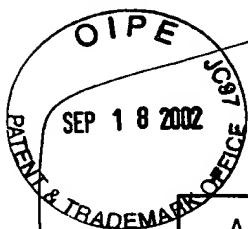


Fig. 32A



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4300B

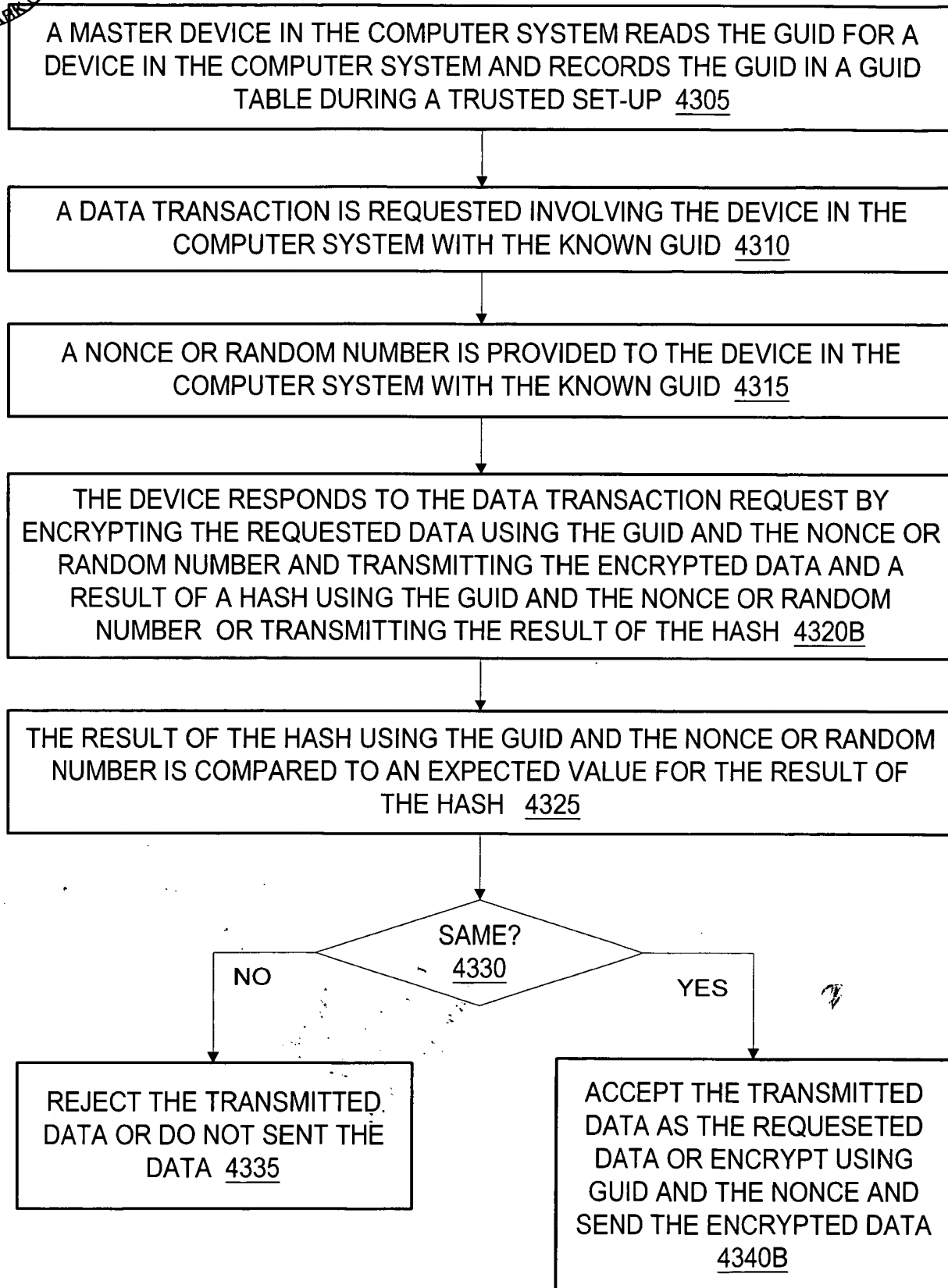
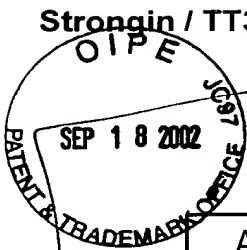


Fig. 32B



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4300C

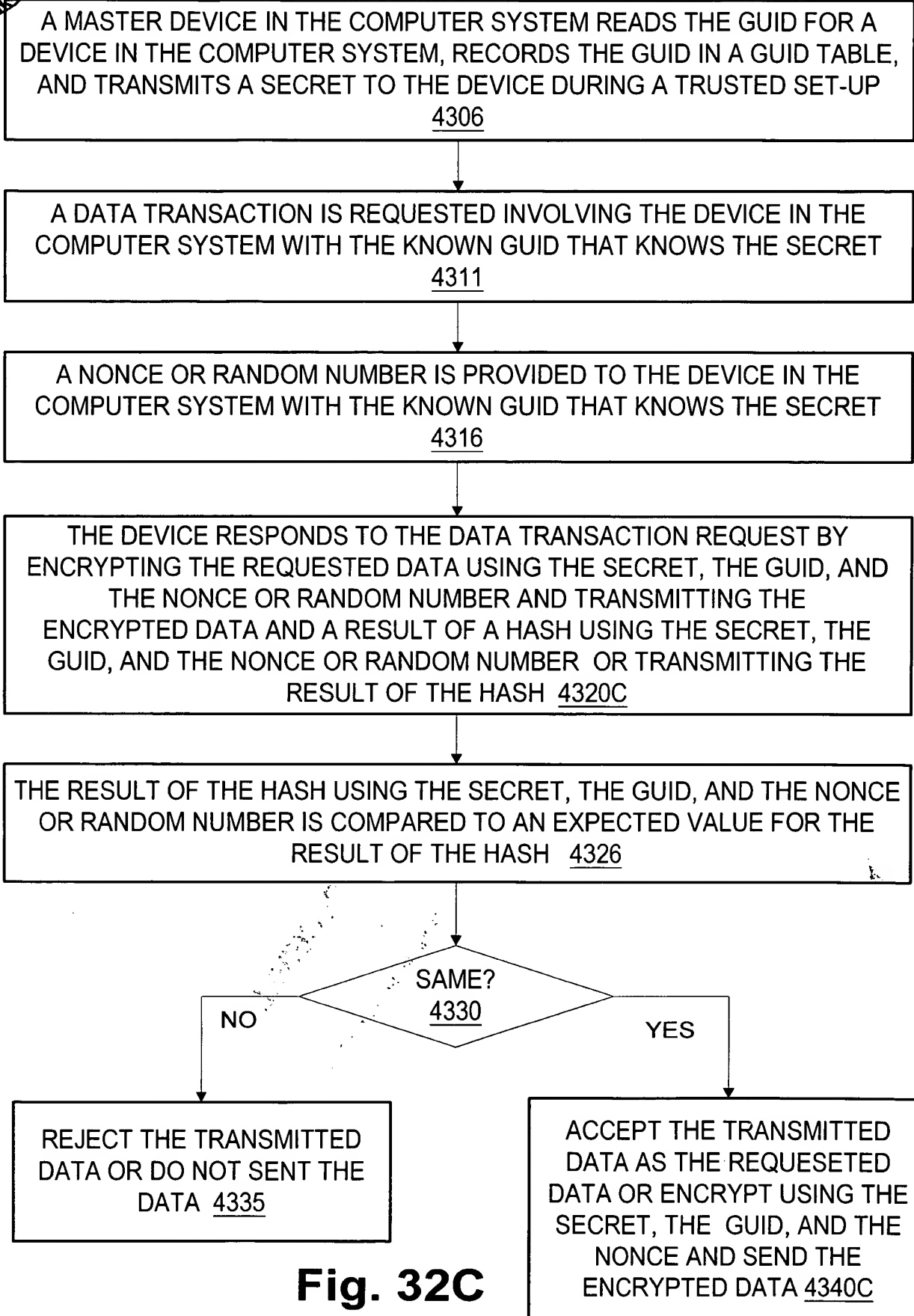


Fig. 32C

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4400

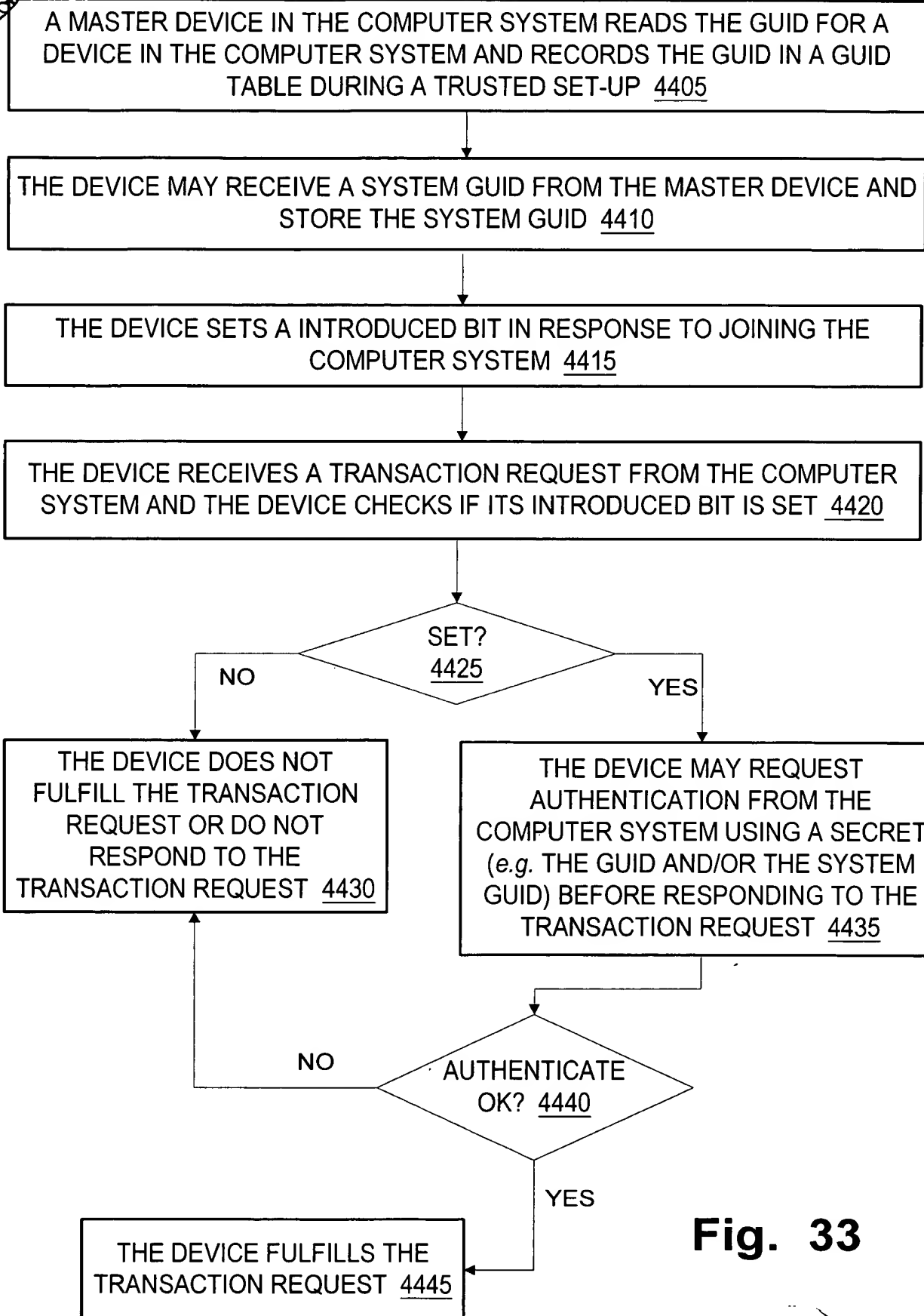


Fig. 33



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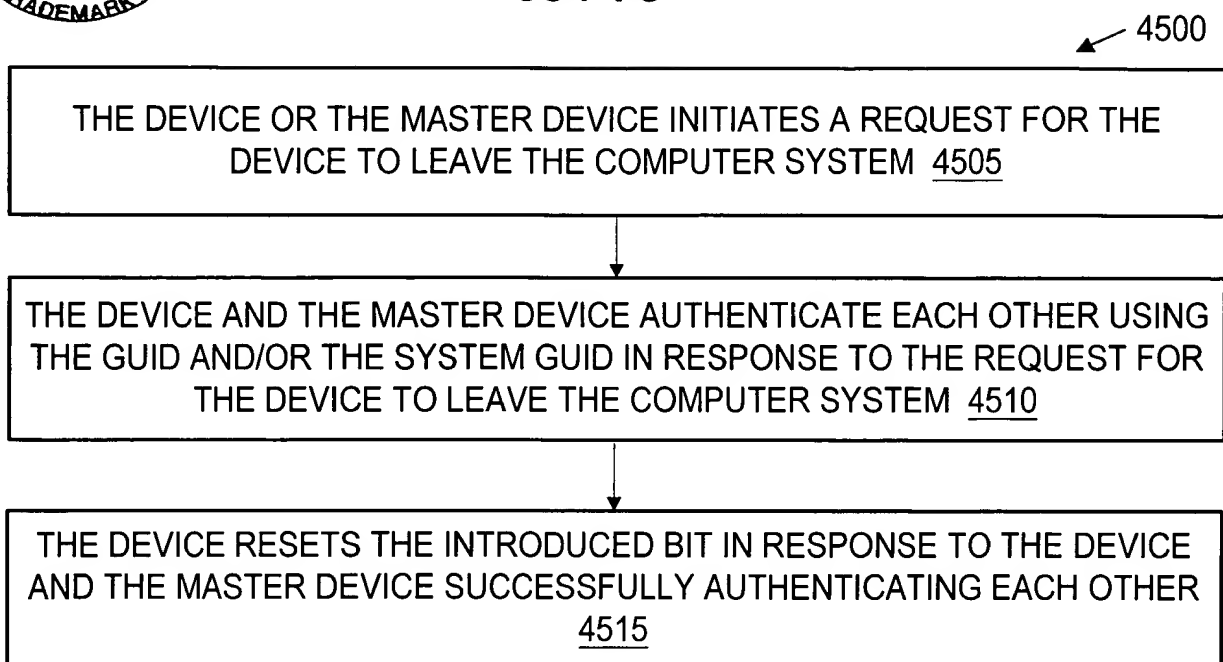


Fig. 34

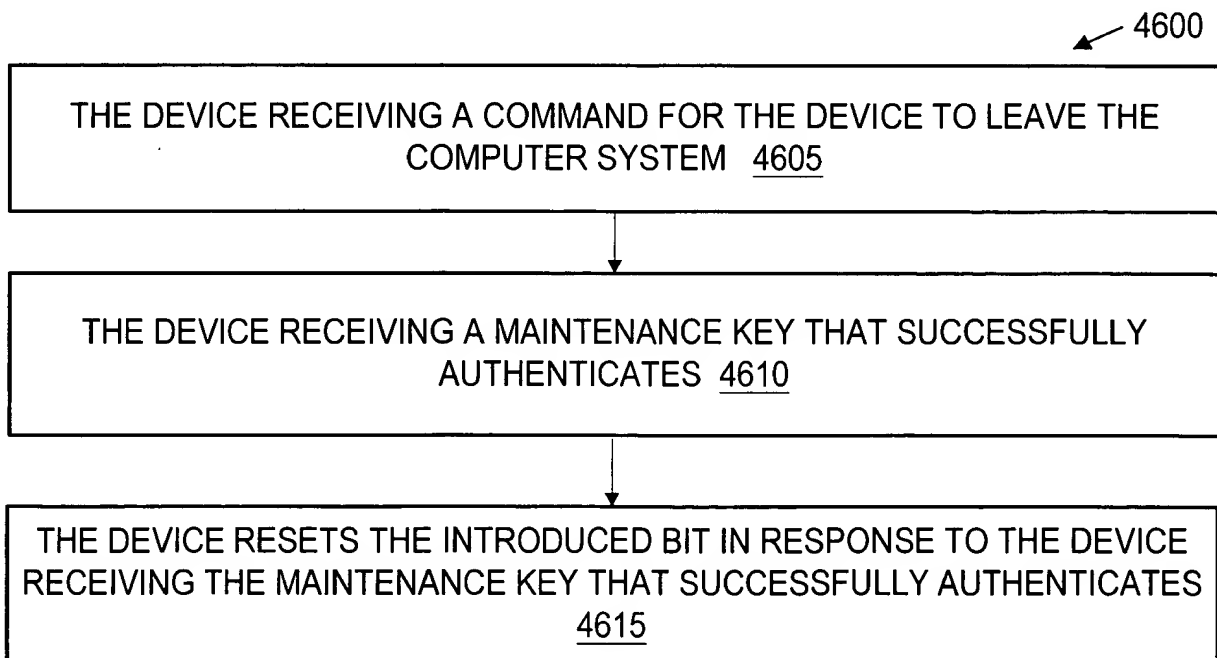


Fig. 35



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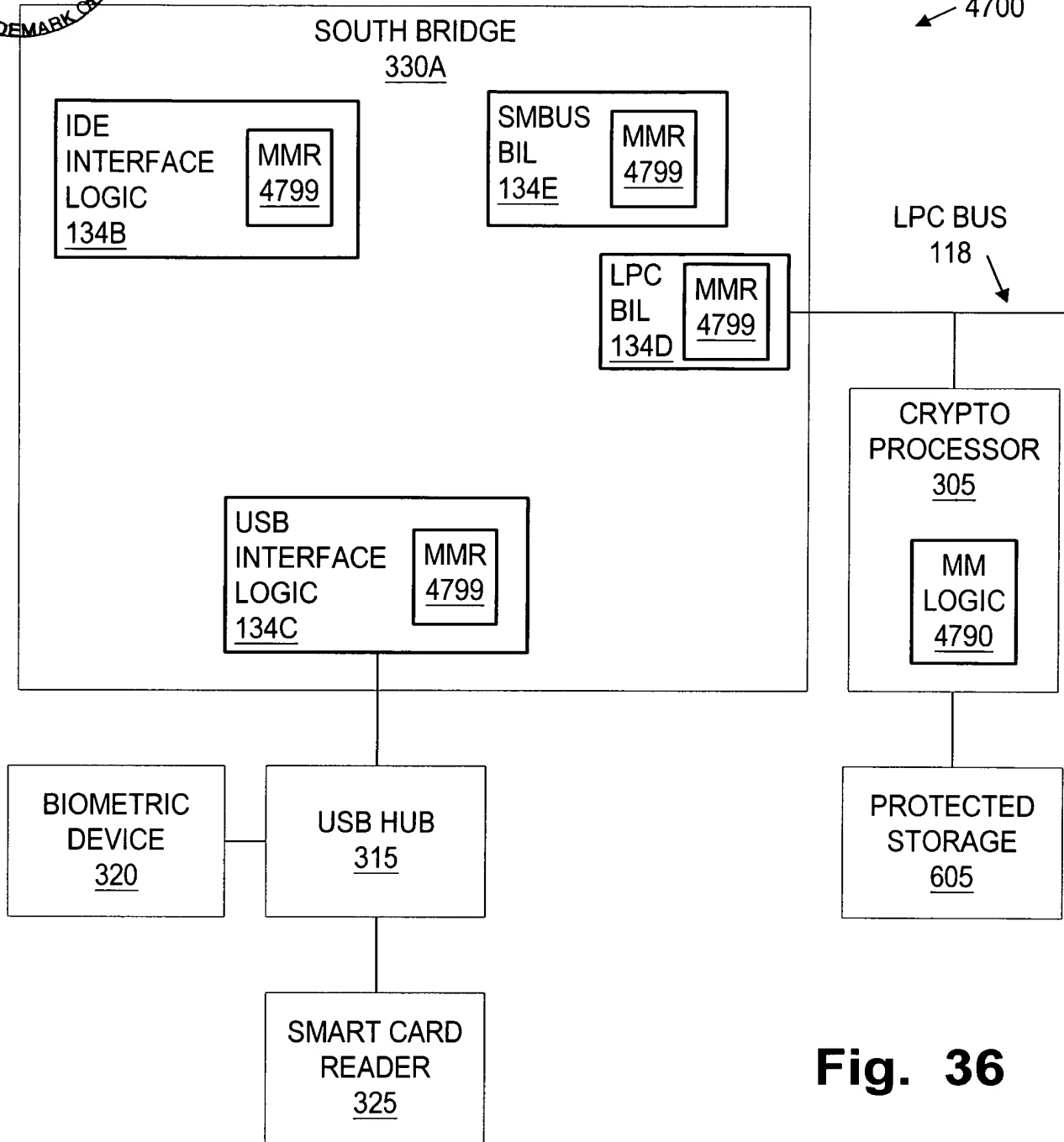
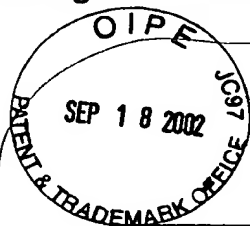


Fig. 36



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4800

TRANSMIT A MASTER MODE SIGNAL TO BUS INTERFACE LOGIC CONNECTED BETWEEN MASTER MODE LOGIC AND A DATA INPUT DEVICE, WHERE THE BUS INTERFACE LOGIC INCLUDES A MASTER MODE REGISTER 4805

SET A MASTER MODE BIT IN THE MASTER MODE REGISTER(S) TO ESTABLISH SECURE TRANSMISSION CHANNEL BETWEEN THE MASTER MODE LOGIC AND THE DATA INPUT DEVICE OUTSIDE THE OPERATING SYSTEM OF THE COMPUTER SYSTEM 4810

THE MASTER MODE LOGIC AND THE DATA INPUT DEVICE EXCHANGE DATA OUTSIDE THE OPERATING SYSTEM OF THE COMPUTER SYSTEM THROUGH THE BUS INTERFACE LOGIC(S) THAT INCLUDE THE MASTER MODE REGISTER 4815

THE MASTER MODE LOGIC FLUSHES THE BUFFERS OF THE BUS INTERFACE LOGIC(S) THAT INCLUDE THE MASTER MODE REGISTER AFTER CONCLUDING THE DATA TRANSMISSIONS 4820

THE MASTER MODE LOGIC SIGNALS THE BUS INTERFACE LOGIC(S) TO UNSET THE MASTER MODE BITS AFTER FLUSHING THE BUFFERS OF THE BUS INTERFACE LOGIC(S) THAT INCLUDE THE MASTER MODE REGISTER 4825

Fig. 37



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4900A

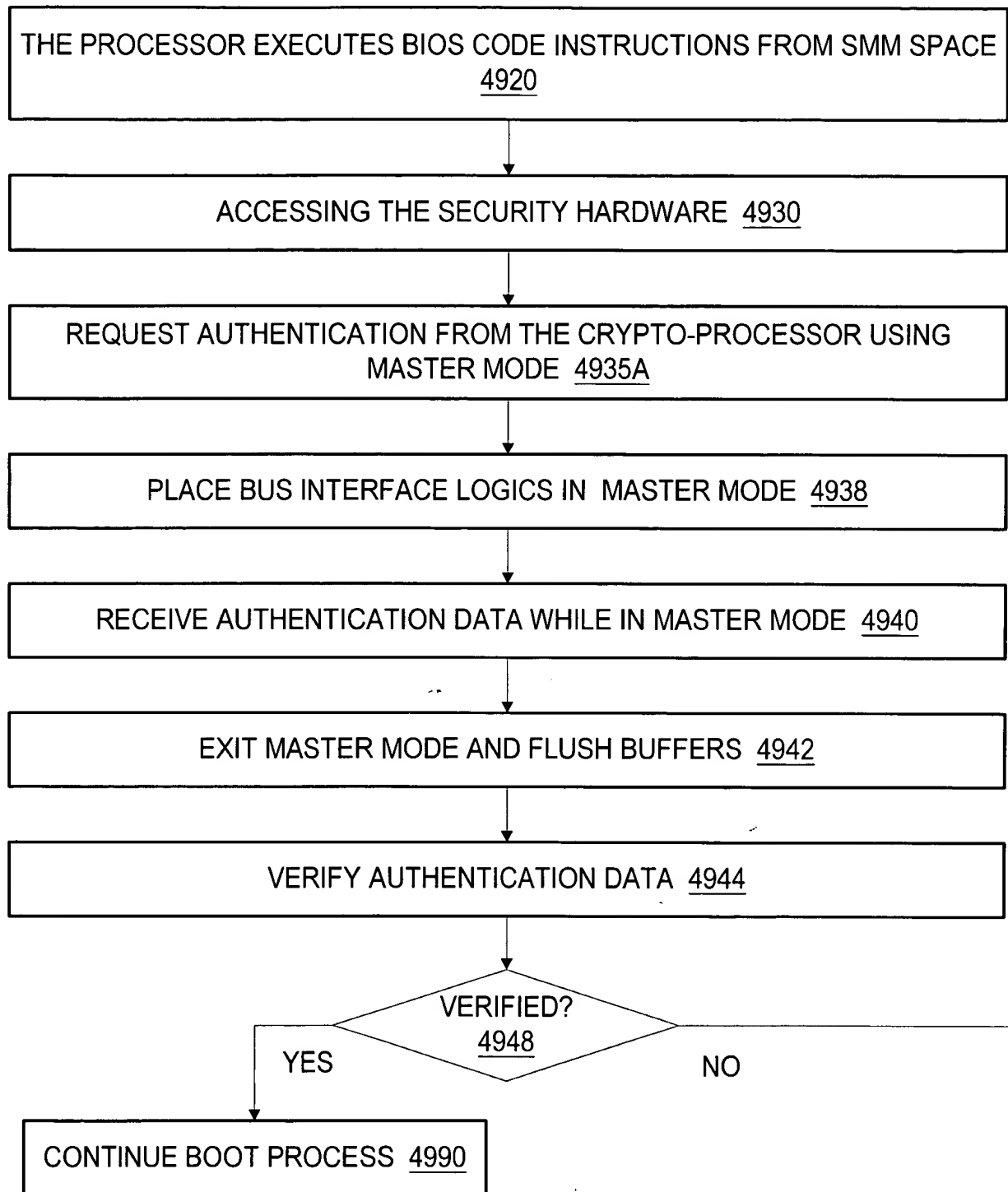
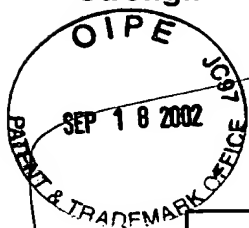


Fig. 38A



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4900B

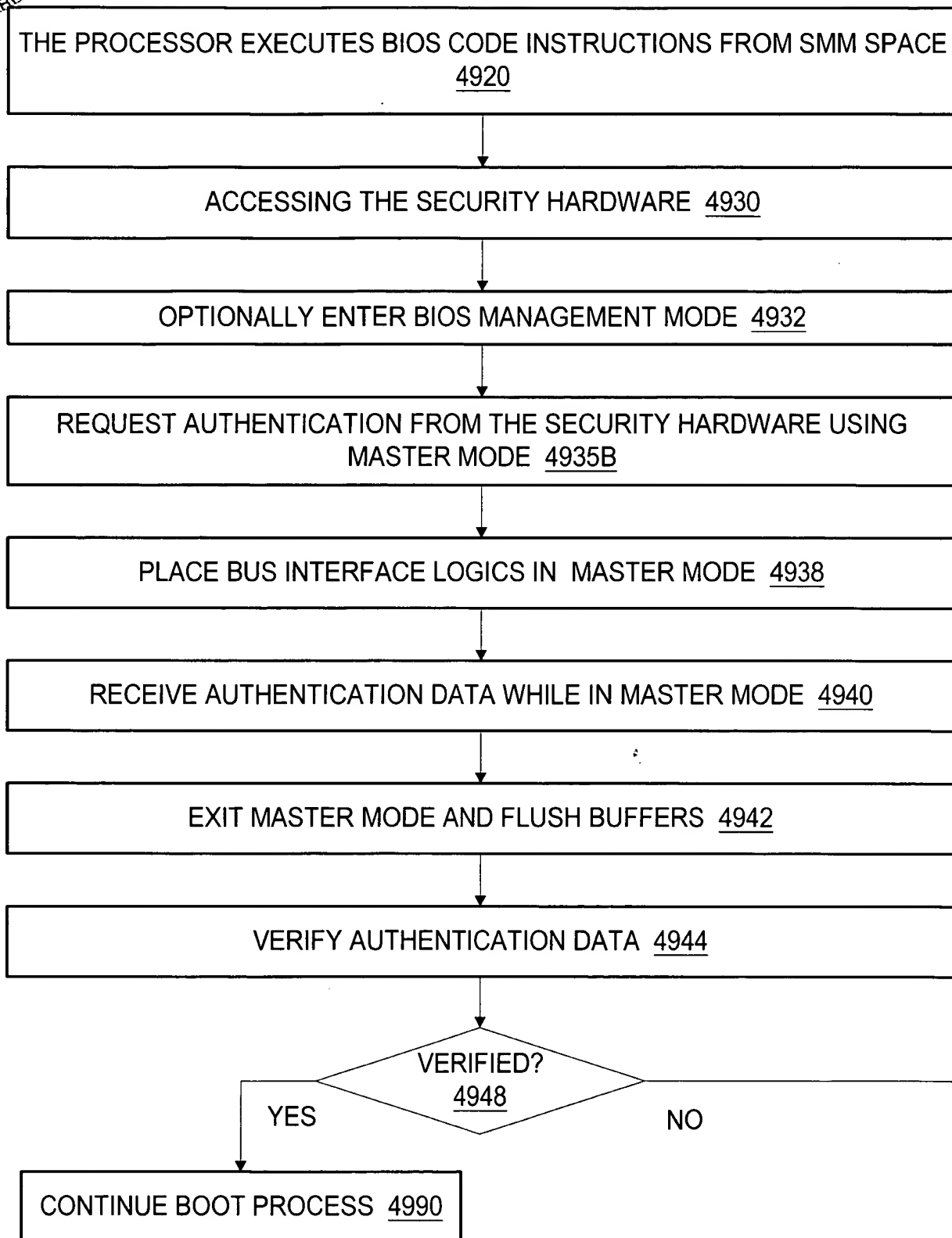
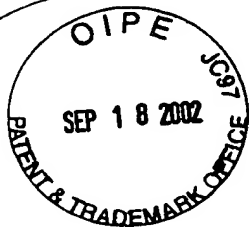


Fig. 38B



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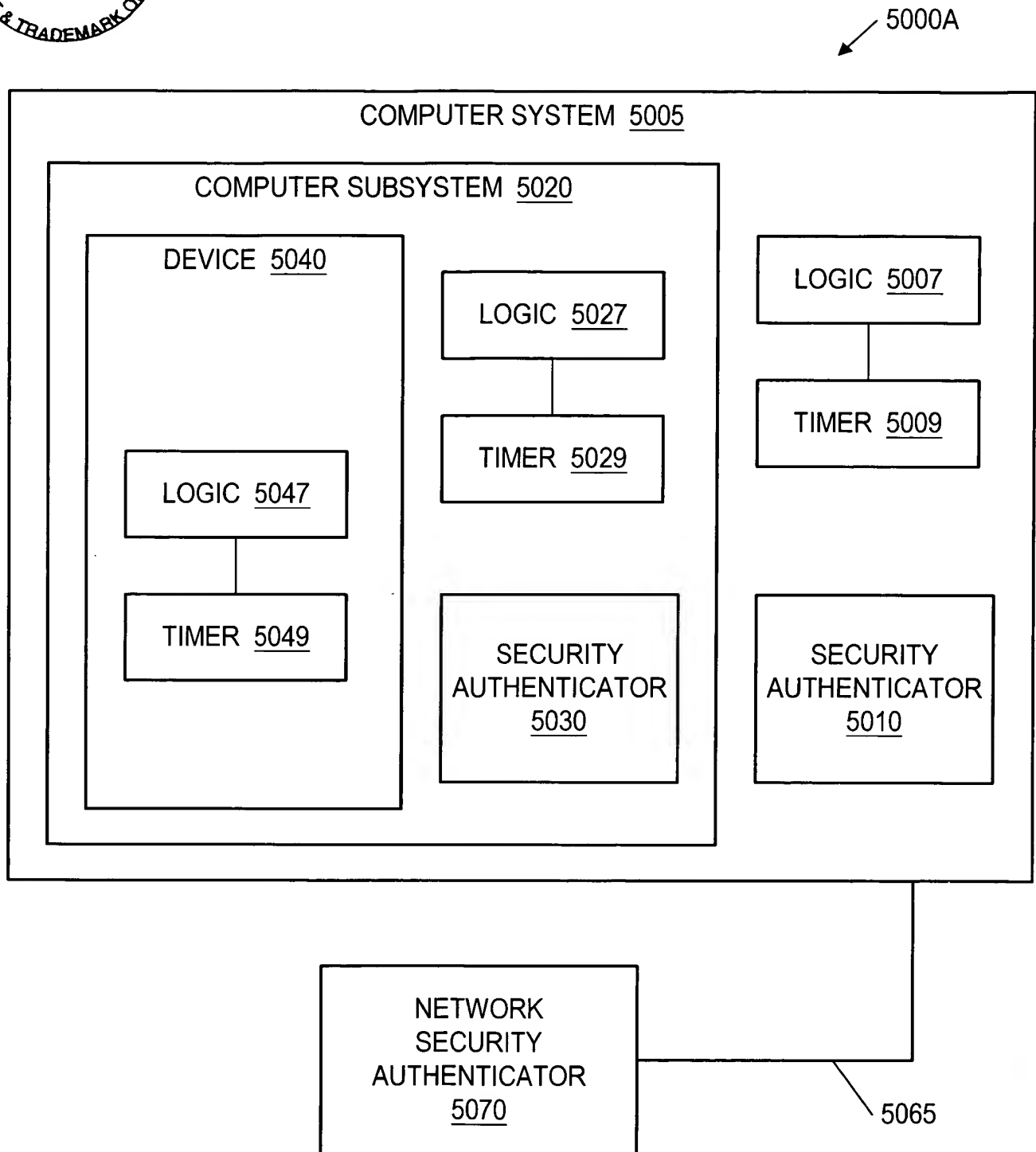
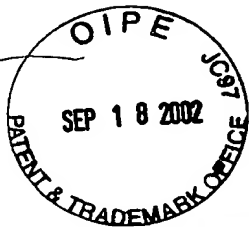


Fig. 39A



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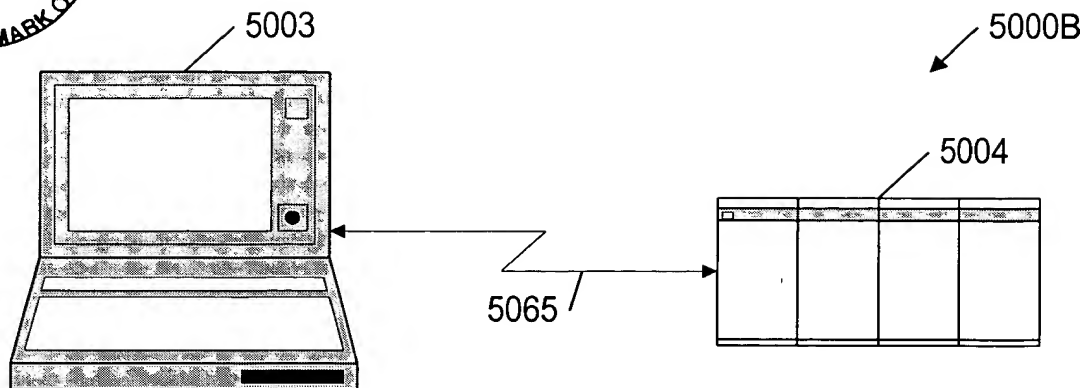


Fig. 39B

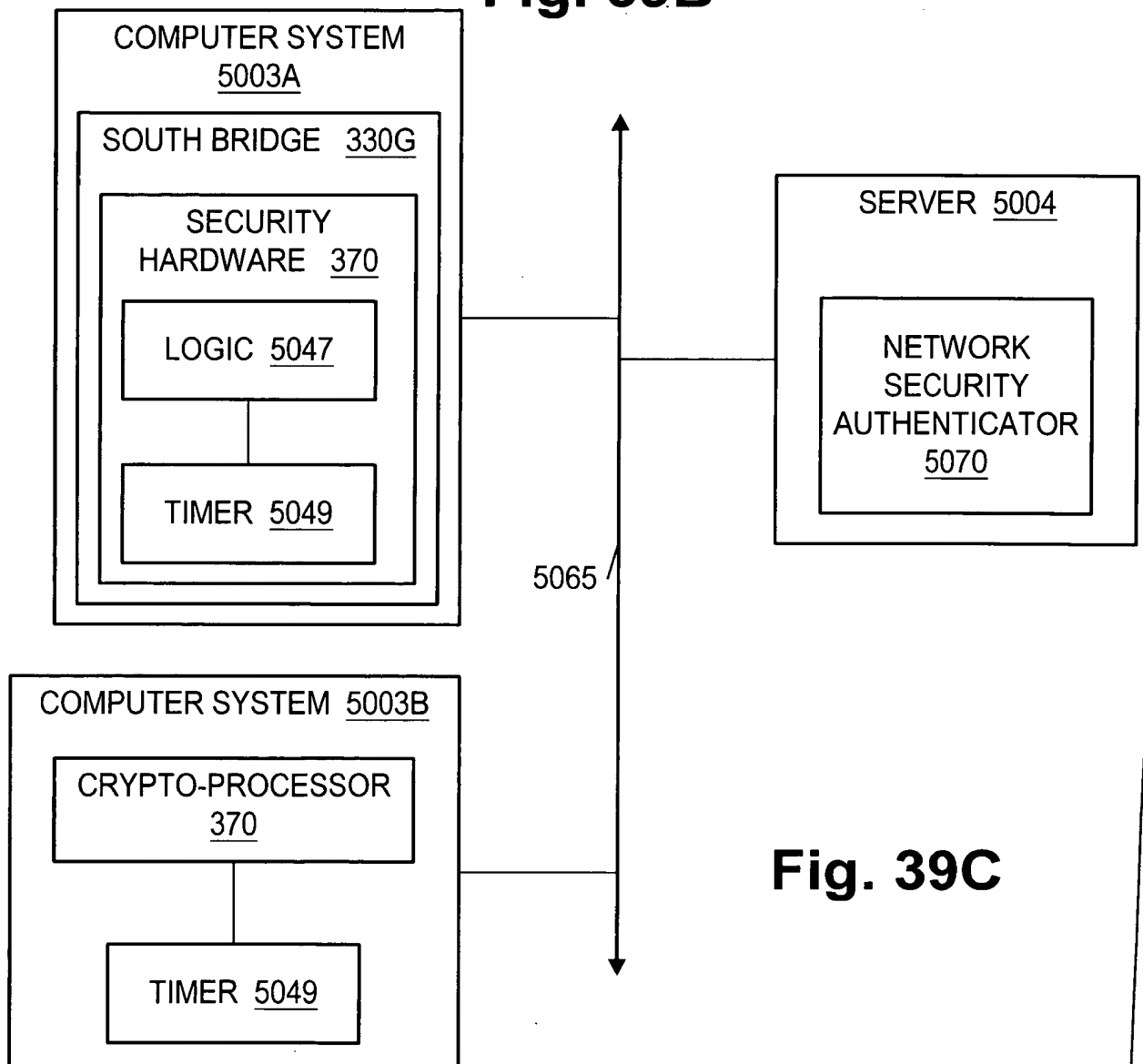
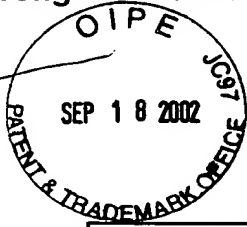


Fig. 39C



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5100A

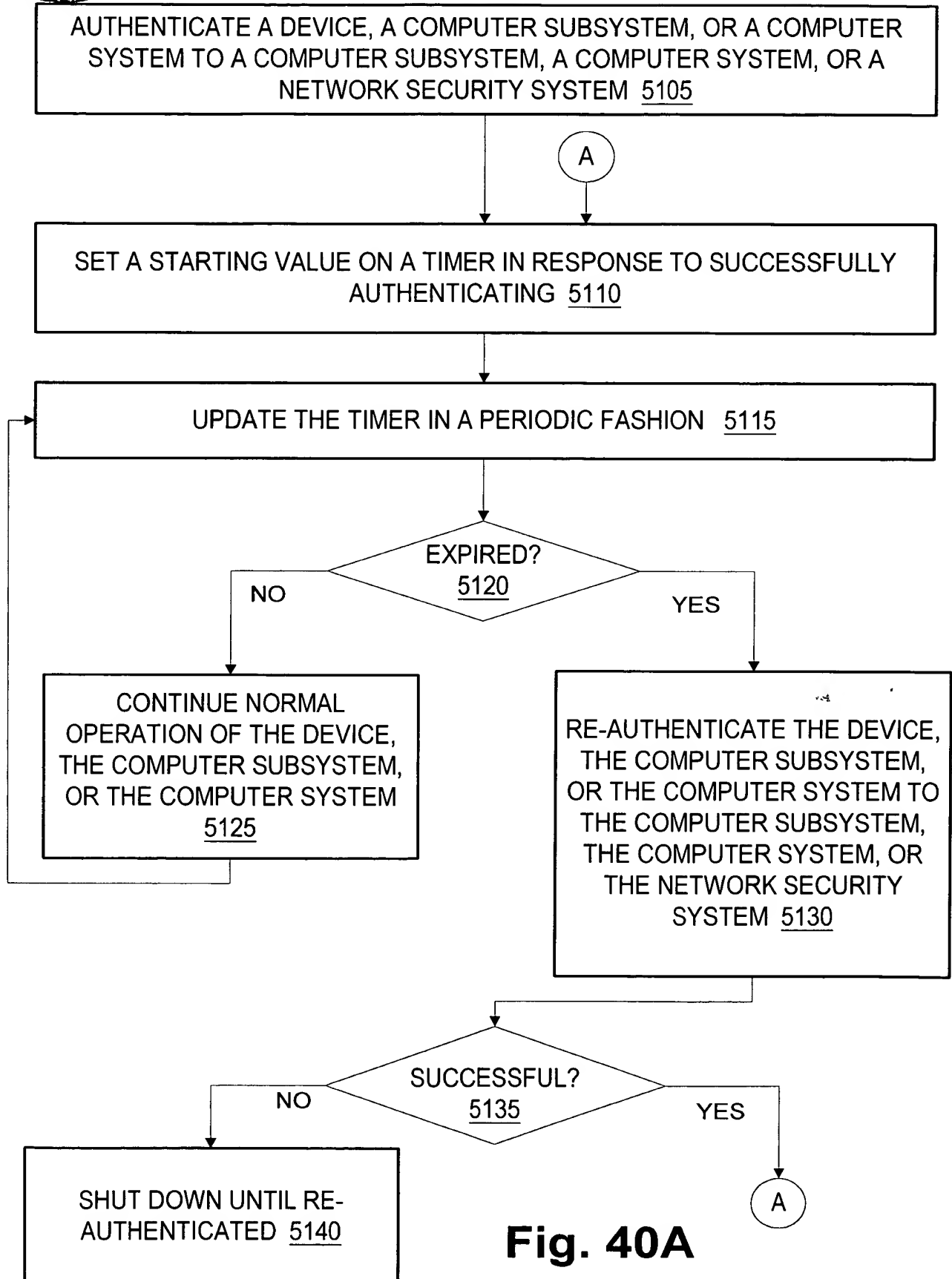


Fig. 40A

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5100B

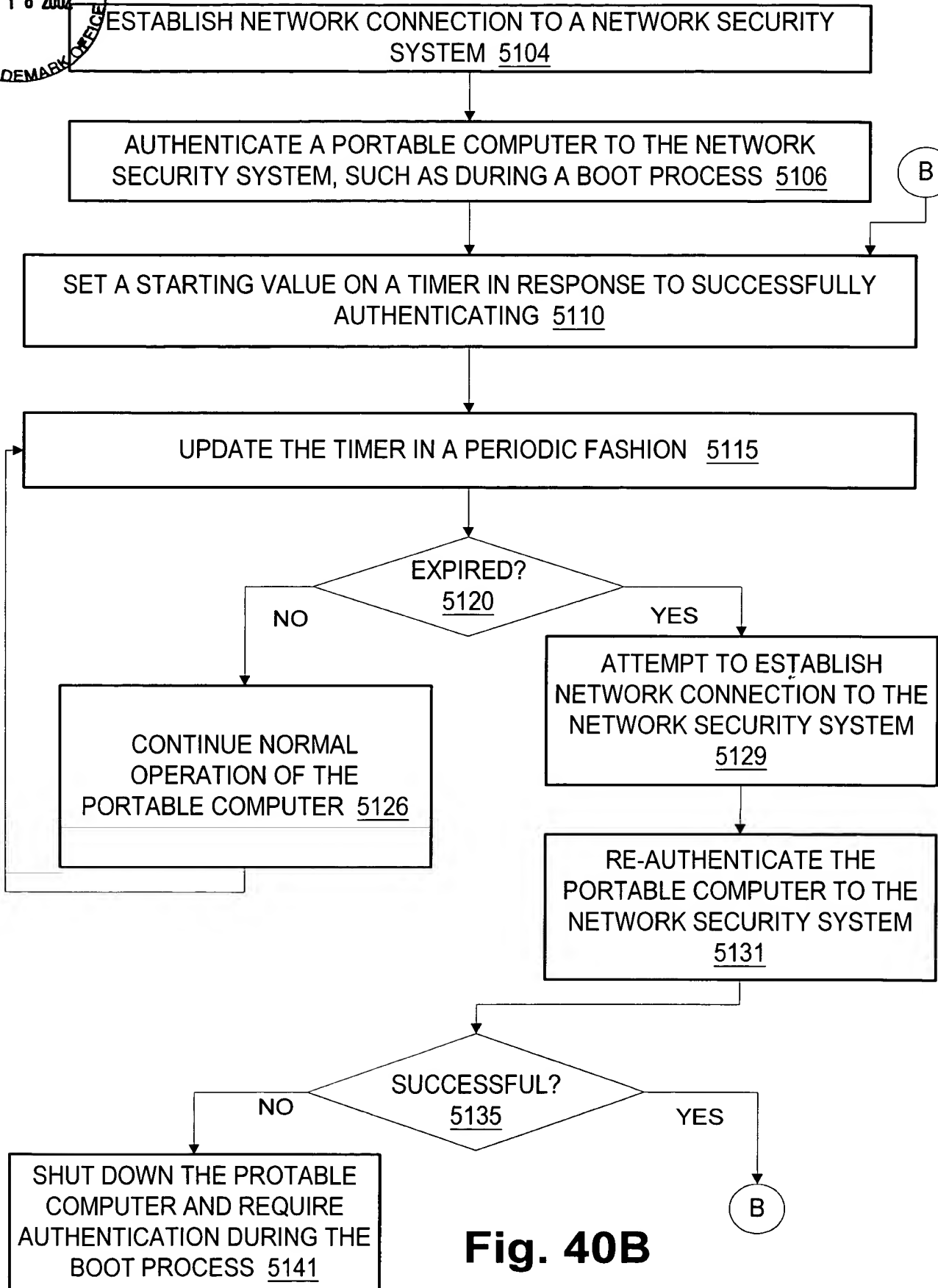


Fig. 40B



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5200

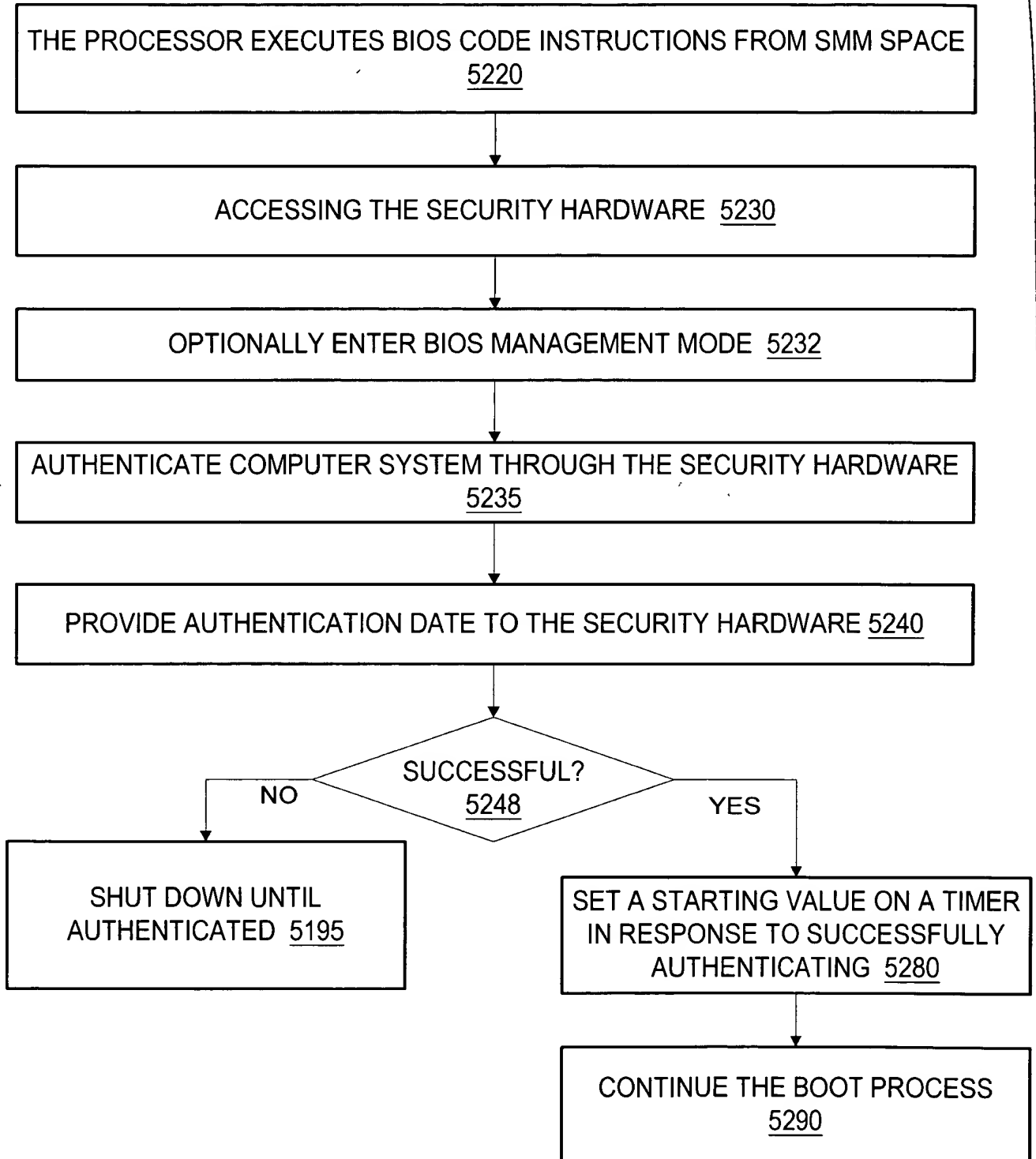


Fig. 41



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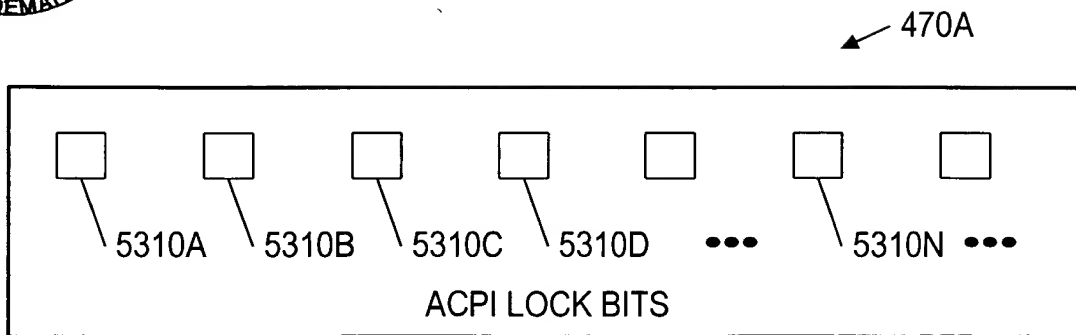


Fig. 42A

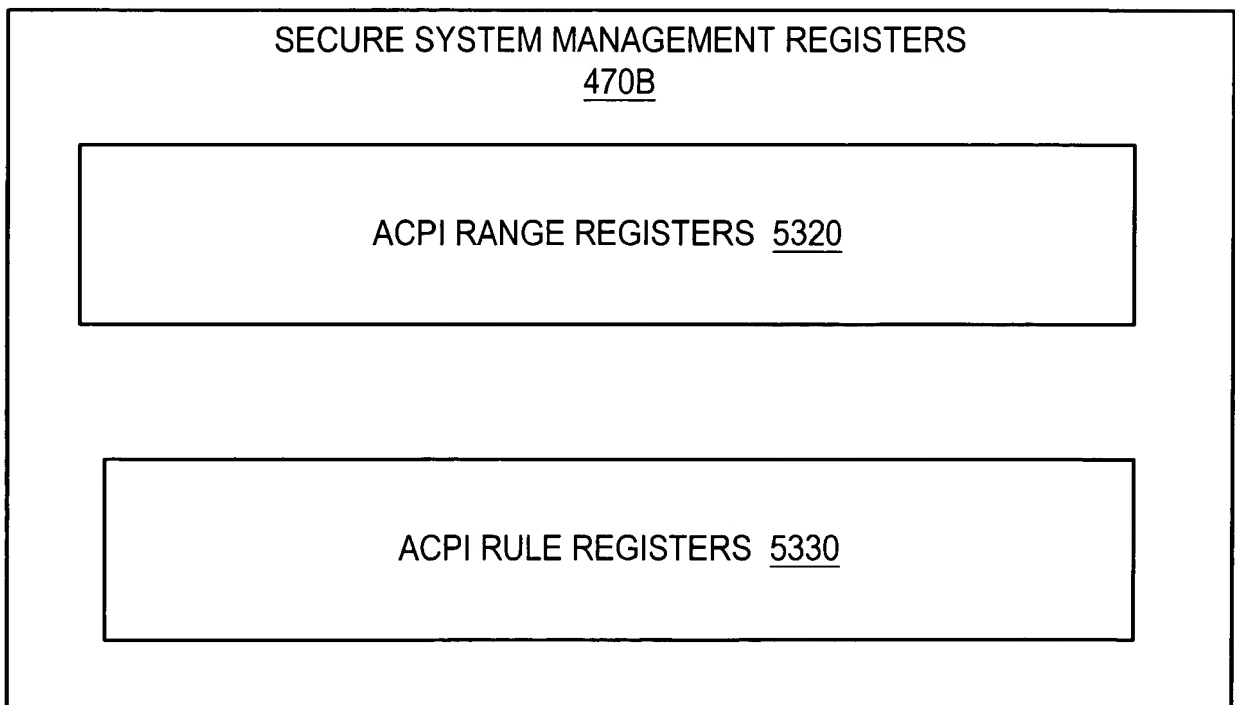


Fig. 42B